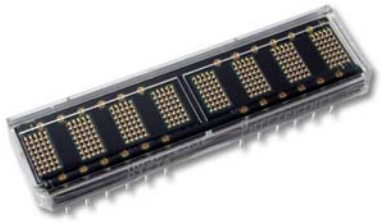
Data Sheet

HDSP-253x Series

Eight Character 5-mm Smart Alphanumeric Display



Description

The Broadcom® HDSP-253x is ideal for applications where displaying eight or more characters of dot matrix information in an aesthetically pleasing manner is required. These devices are eight-digit, 5 x 7 dot matrix, alphanumeric displays. The 5.0-mm (0.2 inch) high characters are packaged in a 0.300-inch (7.62 mm) 30-pin DIP. The onboard CMOS IC has the ability to decode 128 ASCII characters, which are permanently stored in ROM. In addition, 16 programmable symbols can be stored in onboard RAM. Seven brightness levels provide versatility in adjusting the display intensity and power consumption. The HDSP-253x is designed for standard microprocessor interface techniques. The display and special features are accessed through a bidirectional eight-bit data bus.

CAUTION! Normal CMOS handling precautions should be observed to avoid static discharge.

Features

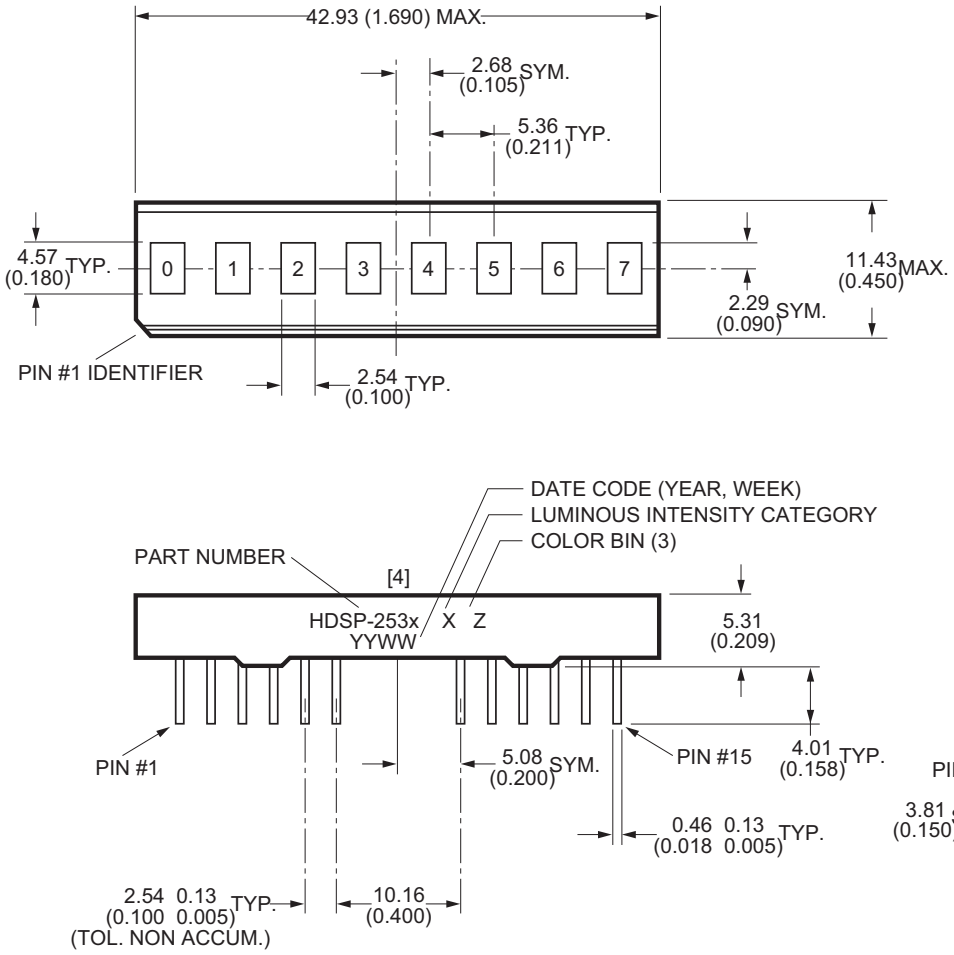
- XY stackable
- 128 character ASCII decoder
- Programmable functions
- 16 user definable characters
- Multilevel dimming and blanking
- TTL compatible CMOS IC
- Wave solderable

Applications

- Avionics
- Computer peripherals
- Industrial instrumentation
- Medical equipment
- Portable data entry devices
- Telecommunications
- Test equipment

Package Dimensions

Figure 1: HDSP-253x Package Dimensions



PIN FUNCTION ASSIGNMENT TABLE

PIN #	FUNCTION	PIN #	FUNCTION
1	RST	16	GND (SUPPLY)
2	FL	17	THERMAL TEST
3	A0	18	GND (LOGIC)
4	A1	19	RD
5	A2	20	D0
6	A3	21	D1
7	NO PIN	22	NO PIN
8	NO PIN	23	NO PIN
9	NO PIN	24	NO PIN
10	A4	25	D2
11	CLS	26	D3
12	CLK	27	D4
13	WR	28	D5
14	CE	29	D6
15	V_{DD}	30	D7

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, TOLERANCE ON DIMENSIONS IS ±0.25 mm (0.010 INCH).
3. FOR YELLOW AND GREEN DISPLAYS ONLY.
4. MARKING IS ON SIDE OPPOSITE PIN 1.

Device Selection Guide

Deep Red	HER	Orange	Yellow	Green
HDSP-2534	HDSP-2532	HDSP-2530	HDSP-2531	HDSP-2533

Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD} to Ground[a]	–0.3V to 7.0V
Operating Voltage, V_{DD} to Ground[b]	5.5V
Input Voltage, Any Pin to Ground	–0.3V to V_{DD} + 0.3V
Free Air Operating Temperature Range, T_A[c]	–40°C to +85°C
Relative Humidity (Noncondensing)	85%
Storage Temperature Range, T_S	–55°C to +100°C
Soldering Temperature [1.59 mm (0.063 in.) Below Body]	
Solder Dipping	260°C for 5 secs
Wave Soldering	250°C for 3 secs
ESD Protection at 1.5 kΩ, 100 pF	4 kV (each pin)

a. Maximum voltage is with no LEDs illuminated.

b. 20 dots ON in all locations at full brightness.

c. See the Thermal Considerations section for information about operation in high temperature ambients.

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Optical Characteristics at 25°C[1]

V_{DD} = 5.0V at full brightness.

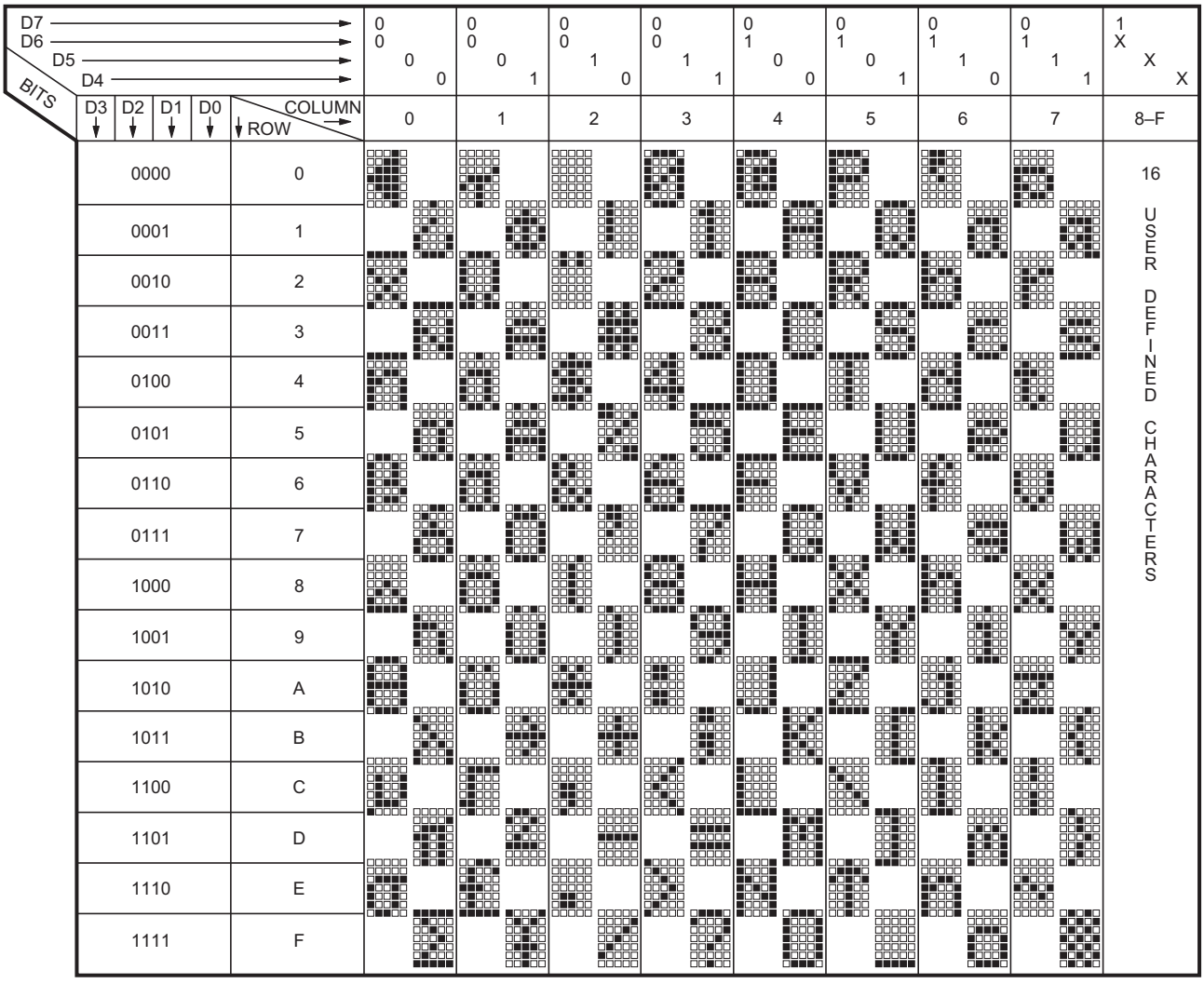
LED Color	Part Number	Luminous Intensity Character Average (#) I_V (mcd)		Peak Wavelength I_{PEAK} (nm)	Dominant Wavelength[a] I_d (nm)
		Min.	Typ.	Typ.	Typ.
Deep Red	HDSP-2534	5.1	63	645	637
High Efficiency Red	HDSP-2532	2.5	7.5	635	626
Orange	HDSP-2530	2.5	7.5	600	602
Yellow	HDSP-2531	2.5	7.5	583	585
Green	HDSP-2533	2.5	7.5	568	574

a. Dominant wavelength, I_d, is derived from the CIE chromaticity diagram, and represents the single wavelength that defines the color of the device.

1. Refers to the initial case temperature of the device immediately prior to measurement.

ASCII Character Set

Figure 2: ASCII Character Set



Electrical Characteristics over Operating Temperature Range

4.5 < V_{DD} < 5.5 unless otherwise specified.

Parameter	Symbol	Min.	25°C Typ.[a]	25°C Max.[a]	Max.	Unit	Test Conditions
Input Leakage (Input without Pull-up)	I_I	–1.0	—	—	1.0	mA	V_{IN} = 0 to V_{DD}, Pins CLK, D_0 to D_7, A_0 to A_4
Input Current (Input with Pull-up)	I_{IP}	–30	–11	–18	0	mA	V_{IN} = 0 to V_{DD}, Pins CLS, $\overline{RST}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, $\overline{FL}$
I_{DD} Blank	I_{DD}(BL)	—	0.5	3.0	4.0	mA	V_{IN} = V_{DD}
I_{DD}8 Digits 12 Dots/Char[b,c,d] (Deep Red)	I_{DD}(V)	—	230	295	390	mA	*V* On in All 8 locations
I_{DD}8 Digits 20 Dots/Char[b,c,d] (Deep Red)	I_{DD}(#)	—	330	410	480	mA	# On in all 8 locations
I_{DD}8 Digits 12 Dots/Char[b,c,d] (All Colors Except Deep Red)	I_{DD}(V)	—	200	255	330	mA	*V* On in all 8 locations
I_{DD}8 Digits 20 Dots/Char[b,c,d] (All Colors Except Deep Red)	I_{DD}(#)	—	300	370	430	mA	# On in all 8 locations
Input Voltage High	V_{IH}	2.0	—	—	V_{DD} +0.3V	V	
Input Voltage Low	V_{IL}	GND –0.3V	—	—	0.8	V	
Output Voltage High	V_{OH}	2.4	—	—	—	V	V_{DD} = 4.5V, I_{OH} = –40 µA
Output Voltage Low D_0 to D_7	V_{OL}	—	—	—	0.4	V	V_{DD} = 4.5V, I_{OL} = 1.6 mA
Output Voltage Low CLK	V_{OL}	—	—	—	0.4	V	V_{DD} = 4.5V, I_{OL} = 40 µA
Thermal Resistance IC Junction-to-PIN	$R\theta_{J\text{-}PIN}$	—	16	—	—	°C/W	Measured at Pin 17

a. V_{DD} = 5.0V.

b. See the Thermal Considerations section for information about operation in high temperature ambients.

c. Average I_{DD} measured at full brightness. See Table 1 in Control Word Register for I_{DD} at lower brightness levels. Peak I_{DD} = 28/15 × I_{DD}(#).

d. Maximum I_{DD} occurs at –55°C.

AC Timing Characteristics over Temperature Range

V_{DD} = 4.5V to 5.5V unless otherwise specified.

Reference Number	Symbol	Description	Min.[a]	Unit
1	t_{ACC}	Display Access Time		ns
		Write	210	
		Read	230	
2	t_{ACS}	Address Setup Time to Chip Enable	10	ns
3	t_{CE}	Chip Enable Active Time[b,c]		ns
		Write	140	
		Read	160	
4	t_{ACH}	Address Hold Time to Chip Enable	20	ns
5	t_{CER}	Chip Enable Recovery Time	60	ns
6	t_{CES}	Chip Enable Active Prior to Rising Edge of [b,c]		ns
		Write	140	
		Read	160	
7	t_{CEH}	Chip Enable Hold Time to Rising Edge of Read/ Write Signal[b,c]	0	ns
8	t_W	Write Active Time	100	ns
9	t_{WD}	Data Valid Prior to Rising Edge of Write Signal	50	ns
10	t_{DH}	Data Write Hold Time	20	ns
11	t_R	Chip Enable Active Prior to Valid Data	160	ns
12	t_{RD}	Read Active Prior to Valid Data	75	ns
13	t_{DF}	Read Data Float Delay	10	ns
	t_{RC}	Reset Active Time[d]	300	ns

a. Worst-case values occur at an IC junction temperature of 125°C.

b. For designers who do not need to read from the display, the Read line can be tied to V_{DD} and the Write and Chip Enable lines can be tied together.

c. Changing the logic levels of the Address lines when $\overline{CE}$ = 0 can cause erroneous data to be entered into the Character RAM, regardless of the logic levels of the $\overline{WR}$ and $\overline{RD}$ lines.

d. The display must not be accessed until after 3 clock pulses (110 µs min. using the internal refresh clock) after the rising edge of the reset line.

Symbol	Description	25°C Typical	Min.[a]	Unit
FOSC	Oscillator Frequency	57	28	kHz
FRF[b]	Display Refresh Rate	256	128	Hz
FFL[c]	Character Flash Rate	2	1	Hz
tST[d]	Self-Test Cycle Time	4.6	9.2	s

a. Worst-case values occur at an IC junction temperature of 125°C

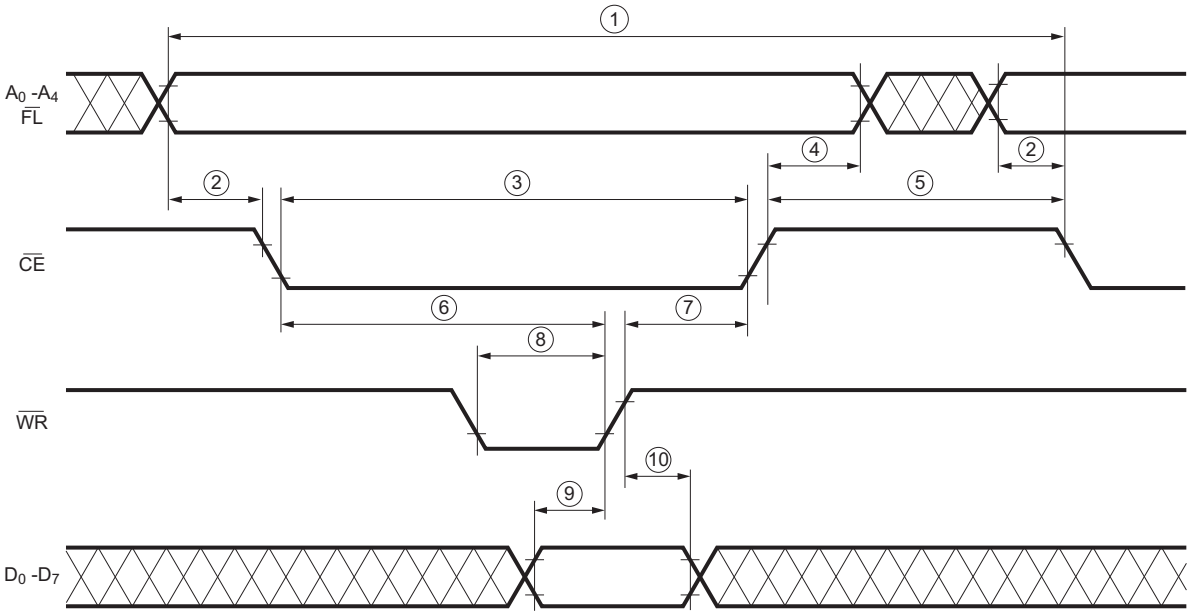
b. $F_{RF} = F_{OSC}/224$.

c. $F_{FL} = F_{OSC}/28{,}672$.

d. $t_{ST} = 262{,}144/F_{OSC}$.

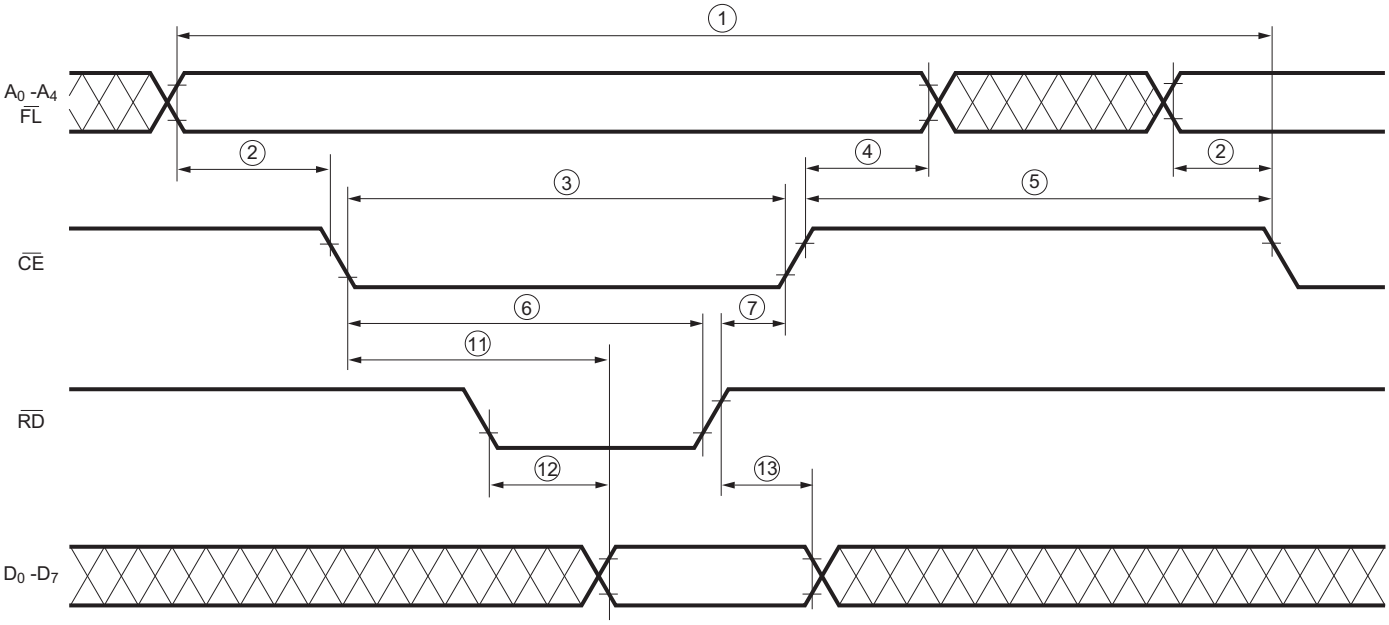
Timing Diagrams

Figure 3: Write Cycle Timing Diagram



INPUT PULSE LEVELS: 0.6V to 2.4V

Figure 4: Read Cycle Timing Diagram



INPUT PULSE LEVELS: 0.6V to 2.4V
OUTPUT REFERENCE LEVELS: 0.6V to 2.2V
OUTPUT LOADING = 1 TTL LOAD AND 100 pF

Electrical Description

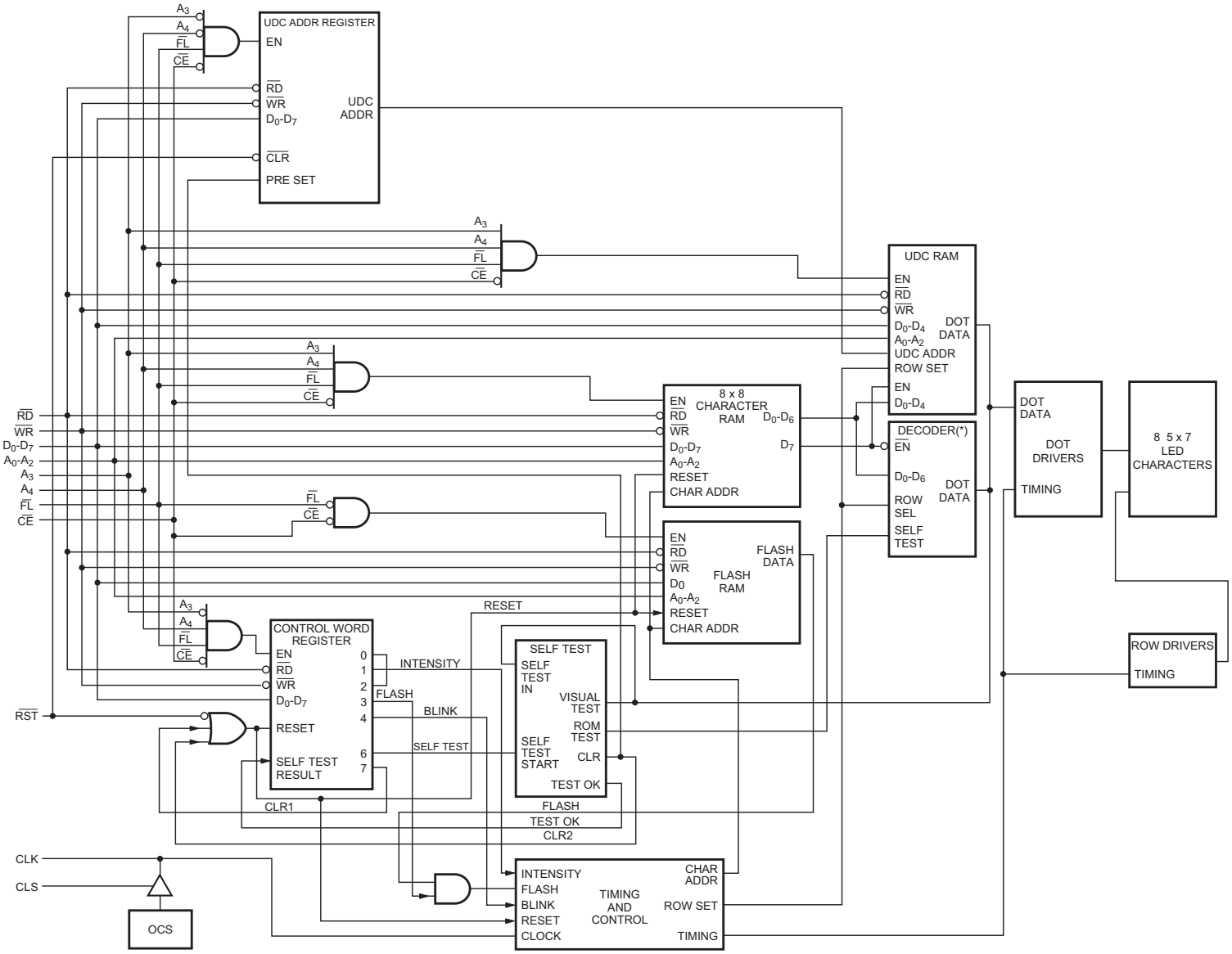
Pin Function	Description
RESET ($\overline{RST}$, pin 1)	Reset initializes the display.
FLASH ($\overline{FL}$, pin 2)	$\overline{FL}$ low indicates an access to the Flash RAM and is unaffected by the state of address lines A_3-A_4.
ADDRESS INPUTS (A_0-A_4, pins 3-6, 10)	Each location in memory has a distinct address. Address inputs (A_0-A_2) select a specific location in the Character RAM, the Flash RAM or a particular row in the User-Defined Character (UDC) RAM. A_3-A_4 are used to select which section of memory is accessed. Refer to the following list for the logic levels needed to access each section of memory. **Logic Levels to Access Memory:** **$\overline{FL}$ / A_4 / A_3 / Section of Memory / A_2 A_1 A_0** 0 / X / X / Flash RAM / Character Address 1 / 0 / 0 / USC Address Register / Don't Care 1 / 0 / 1 / UDC RAM / Row Address 1 / 1 / 0 / Control Word Register / Don't Care 1 / 1 / 1 / Character RAM / Character Address
CLOCK SELECT (CLS, pin 11)	This input is used to select either an internal (CLS = 1) or external (CLS = 0) clock source.
CLOCK INPUT/OUTPUT (CLK, pin 12)	Outputs the master clock (CLS = 1) or inputs a clock (CLS = 0) for slave displays.
WRITE ($\overline{WR}$, pin 13)	Data is written into the display when the $\overline{WR}$ input is low and the $\overline{CE}$ input is low.
CHIP ENABLE ($\overline{CE}$, pin 14)	This input must be at a logic low to read or write data to the display and must go high between each read and write cycle.
READ ($\overline{RD}$, pin 19)	Data is read from the display when the $\overline{RD}$ input is low and the $\overline{CE}$ input is low.
DATA Bus (D0-D7, pins 20, 21, 25-30)	The Data bus is used to read from or write to the display.
GND (SUPPLY) (pin 16)	This is the analog ground for the LED drivers.
GND (LOGIC) (pin 18)	This is the digital ground for internal logic.
V_{DD} (POWER) (pin 15)	This is the positive power supply input.
Thermal Test (pin 17)	This pin is used to measure the IC junction temperature. Do not connect.

Display Internal Block Diagram

Figure 5 shows the internal block diagram of the HDSP-253X display. The CMOS IC consists of an 8-byte Character RAM, an 8-bit Flash RAM, a 128-character ASCII decoder, a 16-character UDC RAM, a UDC Address Register, a Control Word Register, and the refresh circuitry necessary to synchronize the decoding and driving of eight 5 × 7 dot matrix characters. The major user accessible portions of the display are listed here:

- **Character RAM** – This RAM stores either ASCII character data or a UDC RAM address.
- **Flash RAM** – This is a 1 × 8 RAM that stores Flash data.
- **User-Defined Character RAM (UDC RAM)** – This RAM stores the dot pattern for custom characters.
- **User-Defined Character Address Register** – This register is used to provide the address to the UDC RAM when the user is writing or reading a custom character.
- **(UDC Address Register) Control Word Register** – This register allows the user to adjust the display brightness, flash individual characters, blink, self-test or clear the display.

Figure 5: HDSP-253X Internal Block Diagram



Character RAM

Figure 6 shows the logic levels needed to access the HDSP-253X Character RAM. During a normal access, $\overline{CE}$ = 0 and either $\overline{RD}$ = 0 or $\overline{WR}$ = 0. However, erroneous data can be written into the Character RAM if the address lines are unstable when $\overline{CE}$ = 0, regardless of the logic levels of the $\overline{RD}$ or $\overline{WR}$ lines. Address lines A0-A2 are used to select the location in the Character RAM. Two types of data can be stored in each Character RAM location: an ASCII code or a UDC RAM address. Data bit D7 is used to differentiate between the ASCII character and a UDC RAM address. D7 = 0 enables the ASCII decoder and D7 = 1 enables the UDC RAM. D0-D6 are used to input ASCII data, and D0-D3 are used to input a UDC address.

Figure 6: Logic Levels to Access the Character RAM

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	
1	0	0	0	UNDEFINED
		0	1	WRITE TO DISPLAY
		1	0	READ FROM DISPLAY
		1	1	UNDEFINED

CONTROL SIGNALS

$\overline{FL}$	A_4	A_3	A_2	A_1	A_0	
1	1	1	CHARACTER ADDRESS			000 = LEFT MOST 111 = RIGHT MOST

CHARACTER RAM ADDRESS

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	128 ASCII CODE						
1	X	X	X	UDC CODE			

CHARACTER RAM DATA FORMAT

DIG_0	DIG_1	DIG_2	DIG_3	DIG_4	DIG_5	DIG_6	DIG_7
000	001	010	011	100	101	110	111
SYMBOL IS ACCESSED IN LOCATION SPECIFIED BY THE CHARACTER ADDRESS ABOVE							

DISPLAY
0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

UDC RAM and UDC Address Register

Figure 7 shows the logic levels needed to access the UDC RAM and the UDC Address Register. The UDC Address Register is eight bits wide. The lower four bits (D0-D3) are used to select one of the 16 UDC locations. The upper four bits (D4-D7) are not used. Once the UDC address has been stored in the UDC Address Register, the UDC RAM can be accessed. To completely specify a 5 × 7 character requires eight write cycles. One cycle is used to store the UDC RAM address in the UDC Address Register. Seven cycles are used to store dot data in the UDC RAM. Data is entered by rows. One cycle is needed to access each row. Figure 8 shows the organization of a UDC character assuming the symbol to be stored is an F. A0-A2 are used to select the row to be accessed and D0-D4 are used to transmit the row dot data. The upper three bits (D5-D7) are ignored. D0 (least significant bit) corresponds to the right most column of the 5 × 7 matrix and D4 (most significant bit) corresponds to the left most column of the 5 × 7 matrix.

Figure 7: Logic Levels to Access a UDC Character

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	
1	0	0	0	UNDEFINED
		0	1	WRITE TO DISPLAY
		1	0	READ FROM DISPLAY
		1	1	UNDEFINED

CONTROL SIGNALS

$\overline{FL}$	A_4	A_3	A_2	A_1	A_0
1	0	0	X	X	X

UDC ADDRESS REGISTER ADDRESS

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	X	X	X	UDC CODE			

UDC ADDRESS REGISTER DATA FORMAT

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	
1	0	0	0	UNDEFINED
		0	1	WRITE TO DISPLAY
		1	0	READ FROM DISPLAY
		1	1	UNDEFINED

CONTROL SIGNALS

$\overline{FL}$	A_4	A_3	A_2	A_1	A_0	
1	0	1	ROW SELECT			000 = ROW 1 110 = ROW 7

UDC RAM ADDRESS

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	X	X	DOT DATA				

UDC RAM DATA FORMAT — COL 1 … COL 5

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

Figure 8: Data to Load "F"igure into the UDC RAM

COL 1	COL 2	COL 3	COL 4	COL 5		UDC CHARACTER	HEX CODE
D_4 1	D_3 1	D_2 1	D_1 1	D_0 1	ROW 1	• • • • •	1F
1	0	0	0	0	ROW 2	•	10
1	0	0	0	0	ROW 3	•	10
1	1	1	1	0	ROW 4	• • • •	1E
1	0	0	0	0	ROW 5	•	10
1	0	0	0	0	ROW 6	•	10
1	0	0	0	0	ROW 7	•	10
IGNORED							

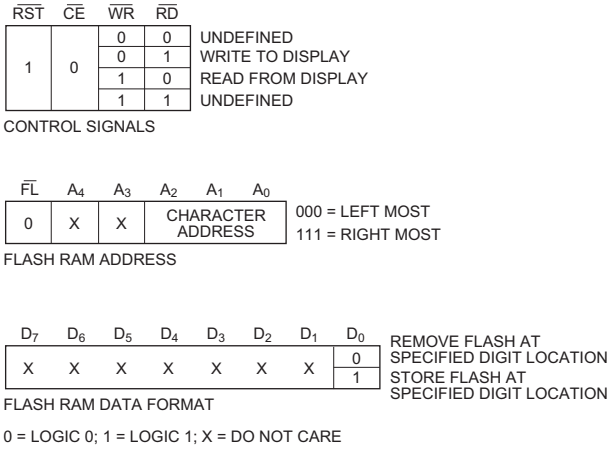
0 = LOGIC 0; 1 = LOGIC 1; * = ILLUMINATED LED

Flash RAM

Figure 9 shows the logic levels needed to access the Flash RAM. The Flash RAM has one bit associated with each location of the Character RAM. The Flash input is used to select the Flash RAM. Address lines A3-A4 are ignored. Address lines A0-A2 are used to select the location in the Flash RAM to store the attribute. D0 is used to store or remove the flash attribute. D0 = 1 stores the attribute and D0 = 0 removes the attribute.

When the attribute is enabled through bit 3 of the Control Word and a 1 is stored in the Flash RAM, the corresponding character will flash at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the flash rate can be calculated by dividing the clock frequency by 28,672.

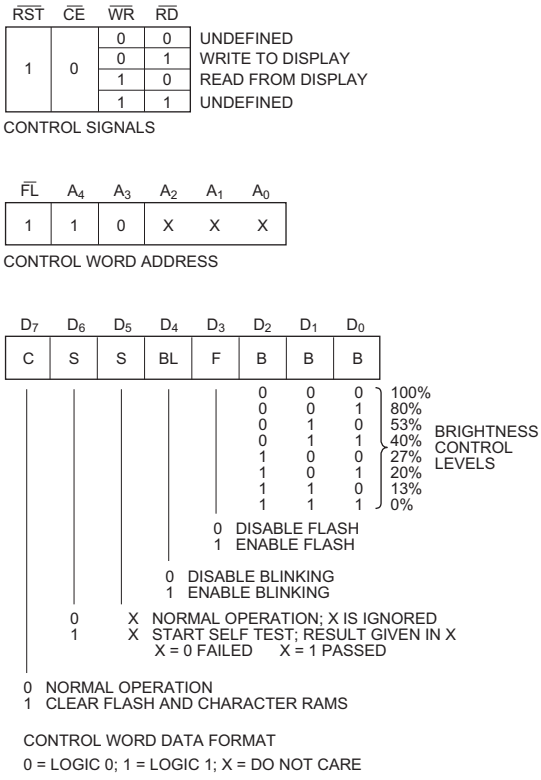
Figure 9: Logic Levels to Access the Flash RAM



Control Word Register

Figure 10 shows how to access the Control Word Register. This is an eight bit register that performs five functions. They are Brightness control, Flash RAM control, Blinking, Self-Test, and Clear. Each function is independent of the others. However, all bits are updated during each Control Word write cycle.

Figure 10: Logic Levels to Access the Control Word Register



Brightness (Bits 0-2)

Bits 0-2 of the Control Word adjust the brightness of the display. Bits 0-2 are interpreted as a three-bit binary code with code (000) corresponding to maximum brightness and code (111) corresponding to a blanked display. In addition to varying the display brightness, bits 0-2 also vary the average value of I_{DD}. I_{DD} can be calculated at any brightness level by multiplying the percent brightness level by the value of I_{DD} at the 100% brightness level. These values of I_{DD} are shown in Table 1.

Table 1: Current Requirements at Different Brightness Levels for All Colors Except AlGaAs

Symbol	D2	D1	D0	% Brightness	V_{DD} = 5.0V 25°C Typ.	Unit
I_{DD} (V)	0	0	0	100	200	mA
	0	0	1	80	160	mA
	0	1	0	53	106	mA
	0	1	1	40	80	mA
	1	0	0	27	54	mA
	1	0	1	20	40	mA
	1	1	0	13	26	mA

Flash Function (Bit 3)

Bit 3 determines whether the flashing character attribute is on or off. When bit 3 is a 1, the output of the Flash RAM is checked. If the content of a location in the Flash RAM is a 1, the associated digit will flash at approximately 2 Hz. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672. If the flash enable bit of the Control Word is a 0, the content of the Flash RAM is ignored. To use this function with multiple display systems, see the Display Reset section.

Blink Function (Bit 4)

Bit 4 of the Control Word is used to synchronize blinking of all eight digits of the display. When this bit is a 1, all eight digits of the display will blink at approximately 2 Hz. The actual rate is dependent on the clock frequency. For an external clock, the blink rate can be calculated by dividing the clock frequency by 28,672.

This function will override the Flash function when it is active. To use this function with multiple display systems, see the Display Reset section.

Self-Test Function (Bits 5, 6)

Bit 6 of the Control Word Register is used to initiate the self-test function. Results of the internal self-test are stored in bit 5 of the Control Word. Bit 5 is a read only bit where bit 5 = 1 indicates a passed self-test and bit 5 = 0 indicates a failed self-test.

Setting bit 6 to a logic 1 will start the self-test function. The built-in self-test function of the IC consists of two internal routines, which exercise major portions of the IC and illuminate all of the LEDs. The first routine cycles the ASCII decoder ROM through all states and performs a checksum on the output. If the checksum agrees with the correct value, bit 5 is set to 1. The second routine provides a visual test of the LEDs using the drive circuitry. This is accomplished by writing checkered and inverse checkered patterns to the display. Each pattern is displayed for approximately 2 seconds.

During the self-test function the display must not be accessed. The time needed to execute the self-test function is calculated by multiplying the clock period by 262,144. For example, assume a clock frequency of 58 kHz, then the time to execute the self-test function frequency is equal to (262,144/58,000) = 4.5 second duration.

At the end of the self test function, the Character RAM is loaded with blanks, the Control Word Register is set to zeros except for bit 5, and the Flash RAM is cleared and the UDC Address Register is set to all ones.

Clear Function (Bit 7)

Bit 7 of the Control Word will clear the Character RAM and the Flash RAM. Setting bit 7 to a 1 will start the clear function.

Three clock cycles (110 ms min. using the internal refresh clock) are required to complete the clear function. The display must not be accessed while the display is being cleared. When the clear function has been completed, bit 7 will be reset to a 0. The ASCII character code for a space (20H) will be loaded into the Character RAM to blank the display, and the Flash RAM will be loaded with 1s. The UDC RAM, the UDC Address Register, and the remainder of the Control Word are unaffected.

Display Reset

Figure 11 shows the logic levels needed to reset the display. The display should be reset on power-up. The external reset clears the Character RAM, Flash RAM, and Control Word, and resets the internal counters. After the rising edge of the Reset signal, three clock cycles (110 ms min. using the internal refresh clock) are required to complete the reset sequence. The display must not be accessed while the display is being reset. The ASCII Character code for a space (20H) will be loaded into the Character RAM to blank the display. The Flash RAM and Control Word Register are loaded with all 0s. The UDC RAM and UDC Address Register are unaffected. All displays that operate with the same clock source must be simultaneously reset to synchronize the Flashing and Blinking functions.

Figure 11: Logic Levels to Reset the Display

$\overline{RST}$	$\overline{CE}$	$\overline{WR}$	$\overline{RD}$	$\overline{FL}$	A_4 -A_0	D_7 -D_0
0	1	X	X	X	X	X

0 = LOGIC 0; 1 = LOGIC 1; X = DO NOT CARE

NOTE:
IF RST, CE, AND WR ARE LOW, UNKNOWN DATA MAY BE WRITTEN INTO THE DISPLAY.

Mechanical Considerations

The HDSP-253X is assembled by die attaching and wire bonding 280 LED chips and a CMOS IC to a thermally conductive printed circuit board. A polycarbonate lens placed over the PCB creates an air gap over the LED wire bonds. A backfill epoxy seals the display package.

Figure 12 shows the proper method to insert the display by hand. To prevent damage to the LED wire bonds, apply pressure uniformly with fingers located at both ends of the part. Using a tool, shown in Figure 13, such as a screwdriver or pliers to push the display into the printed circuit board or socket might damage the LED wire bonds. The force exerted by a screwdriver is sufficient to push the lens into the LED wire bonds. The bent wire bonds cause shorts or opens that result in catastrophic failure of the LEDs.

Figure 12: Proper Method to Manually Insert a Display

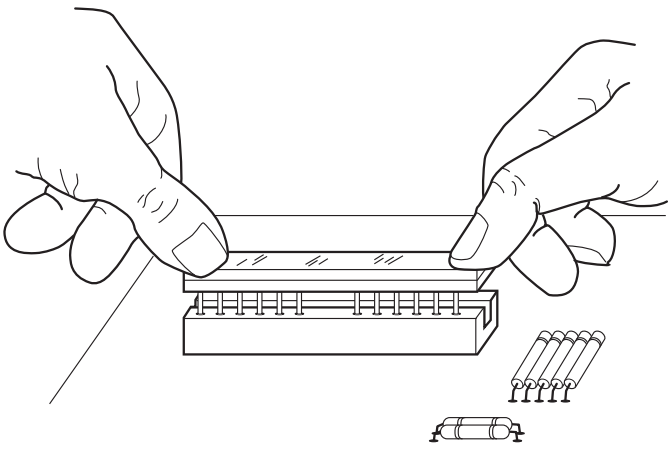
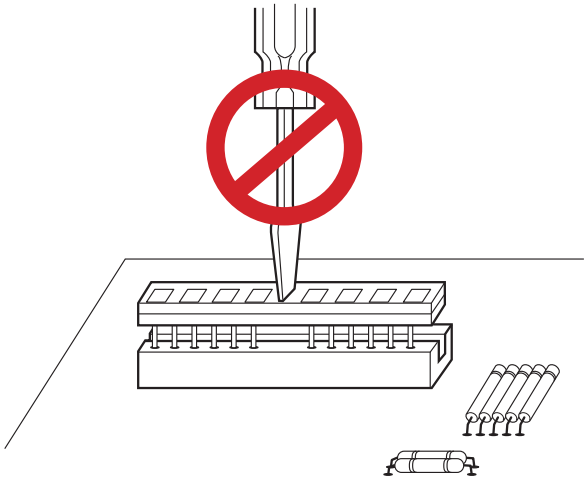


Figure 13: Improper Method to Manually Insert a Display



Thermal Considerations

The HDSP-253X can operate from –40°C to +85°C. The display's low thermal resistance allows heat to flow from the CMOS IC to the 24 package pins. Typically, this heat is conducted through the printed circuit board traces to free air. For most applications, no additional heatsinking is needed. Illuminating all 280 LEDs simultaneously at full brightness is not recommended for continuous operation. However, all 280 LEDs can be illuminated simultaneously at full brightness for 10 seconds at 25°C as a lamp test.

The IC has a maximum allowable junction temperature of 150°C. The IC junction temperature can be calculated with the following equation:

$$T_J MAX = T_A + (P_D \times R\theta_{J\text{-}A})$$

where:

- $T_J MAX$ is the maximum allowable IC junction temperature.
- T_A is the ambient temperature surrounding the display.
- P_D is the power dissipated by the IC.
- $R\theta_{J\text{-}A}$ is the thermal resistance from the IC through the display package and printed circuit board to the ambient.

A typical value for $R\theta_{J\text{-}A}$ is 39°C/W. This value is typical for a display mounted in a socket and covered with a plastic filter. The socket is soldered to a 0.062 in. thick printed circuit board with 0.020 in. wide one-ounce copper traces.

P_D can be calculated as follows:

$$P_D = V_{DD} \times I_{DD}$$

where:

- V_{DD} is the supply voltage and I_{DD} is the supply current.
- V_{DD} can vary from 4.5V to 5.5V.
- I_{DD} changes with V_{DD}, temperature, brightness level, and number of on-pixels.

For Deep Red:

$$I_{DD}(\#) = (83.8 \times V_{DD} - 0.35 \times T_J) \times B \times N/8$$

$$I_{DD}(V) = (63 \times V_{DD} - 0.79 \times T_J) \times B \times N/8$$

For the other colors:

$$I_{DD}(\#) = (75.4 \times V_{DD} - 0.28 \times TJ) \times B \times N/8$$

$$I_{DD}(V) = (54 \times V_{DD} - 0.6 \times TJ) \times B \times N/8$$

where:

- I_{DD} (#) is the supply current using # as the displayed character.
- I_{DD}(V) is the supply current using V as the displayed character.
- T_J is the IC junction temperature.
- B is the percent brightness level.
- N is the number of characters illuminated.

Operation in high temperature ambients might require power derating or heatsinking. Figure 14 shows how to derate the power for an HDSP-253X. You can reduce the power by tighter supply voltage regulation or lowering the brightness level.

Figure 14: Maximum Allowable Power Dissipation vs. Ambient Temperature, $T_J MAX$ = 15°C or 120°C

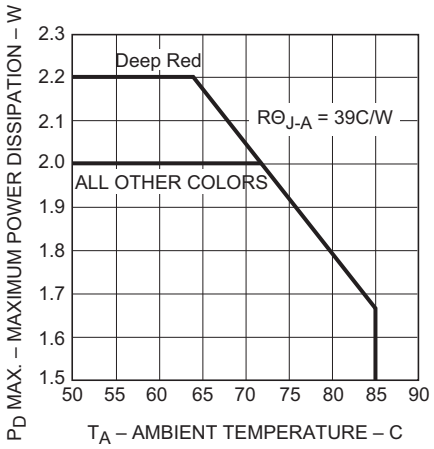


Table 2 and Table 3 show the calculated maximum allowable ambient temperature for several different sets of operating conditions. The worst-case alphanumeric characters (#, @, B) have 20 pixels. Displaying eight 20-pixel characters will not occur in normal operation. Thus, using eight 20-pixel characters to calculate power dissipation will overestimate the power and the IC junction temperature. The average number of pixels per character, supply voltage, brightness level, and number of characters are needed to calculate the power dissipated by the IC. The ambient temperature, power dissipated by the IC, and the thermal resistance are then used to calculate IC junction temperature. The typical alphanumeric character is 15 pixels. For conditions not listed in Table 2 and Table 3, you can calculate the power dissipated by the IC and use Figure 14 to determine the maximum ambient temperature.

Table 2: Maximum Allowable Ambient Temperature for Various Operating Conditions Deep Red

Character	Number of Characters	Brightness Level	V_{DD} V	I_{DD} mA	P_D W	$R\theta_{J-A}$ °C/W	$T_A MAX$ °C
# (20 dots)	8	100%	5.5	408	2.2	39	64
# (20 dots)	8	100%	5.25	387	2.0	39	72
# (20 dots)	8	100%	5.0	366	1.8	39	80
# (20 dots)	7	100%	5.5	357	2.0	39	72
# (20 dots)	6	100%	5.5	306	1.7	39	84
# (20 dots)	8	80%	5.5	327	1.8	39	80
# (20 dots)	8	80%	5.25	310	1.6	39	85
# (20 dots)	8	53%	5.5	216	1.2	39	85
V (12 dots)	8	100%	5.5	228	1.3	39	85

Table 3: Maximum Allowable Ambient Temperature for Various Operating Conditions , All Colors Except Deep Red

Character	Number of Characters	Brightness Level	V_{DD} V	I_{DD} mA	P_D W	$R\theta_{J-A}$ °C/W	$T_A MAX$ °C
# (20 dots)	8	100%	5.5	373	2.0	39	72
# (20 dots)	8	100%	5.25	354	1.9	39	77
# (20 dots)	8	100%	5.0	335	1.67	39	85
# (20 dots)	7	100%	5.5	326	1.8	39	80
# (20 dots)	6	100%	5.5	280	1.5	39	85
# (20 dots)	8	80%	5.5	298	1.6	39	85
V (12 dots)	8	100%	5.5	207	1.1	39	85

NOTE: The actual IC temperature is easy to measure. Pin 17 is thermally and electrically connected to the IC substrate. The thermal resistance from pin 17 to the IC is 16°C/ W. The procedure to measure the IC junction temperature is as follows:

1. Measure V_{DD} and I_{DD} for the display. Measure V_{DD} between pins 15 and 16. Measure the current entering pin 15.
2. Measure the temperature of pin 17 after 45 minutes. Use an electrically isolated thermal couple probe.
3. $T_J(IC) = T_{pin} + V_{DD} \times I_{DD} \times 16°C/ W$.

Ground Connections

Two ground pins are provided to keep the internal IC logic ground clean. The designer can, when necessary, route the analog ground for the LED drivers separately from the logic ground until an appropriate ground plane is available. On long interconnections between the display and the host system, the designer can keep voltage drops on the analog ground from affecting the display logic levels by isolating the two grounds.

The logic ground should be connected to the same ground potential as the logic interface circuitry. The analog ground and the logic ground should be connected at a common ground which can withstand the current induced by the switching LED drivers. When separate ground connections are used, the analog ground can vary from –0.3V to +0.3V with respect to the logic ground. Voltage below –0.3V can cause all dots to be on. Voltage above +0.3V can cause dimming and dot mismatch.

Solder and Post Solder Cleaning

NOTE: Refer to Application Note 1027 for information on soldering and post solder cleaning.

Contrast Enhancement (Filtering)

Refer to Application Note 1015 for information on contrast enhancement.

Intensity Bin Limits for HDSP-2534

Bin	Intensity Range (mcd)[a]	
	Min.	Max.
I	5.12	9.01
J	7.68	13.52
K	11.52	20.28
L	17.27	30.42
M	25.91	45.63
N	38.09	68.45
O	57.13	102.68
P	85.70	154.02

a. Test conditions as specified in the Optical Characteristics at 25°C section.

Intensity Bin Limits for HDSP-253x

Bin	Intensity Range (mcd)[a]	
	Min.	Max.
G	2.50	4.00
H	3.41	6.01
I	5.12	9.01
J	7.68	13.52
K	11.52	20.28

a. Test conditions as specified in the Optical Characteristics at 25°C section.

Color Bin Limits

Color	Bin	Color Range (nm)[a]	
		Min.	Max.
Green	1	576.0	580.0
	2	573.0	577.0
	3	570.0	574.0
	4	567.0	571.0
Yellow	3	581.5	585.0
	4	584.0	587.5
	5	586.5	590.0
	6	589.0	592.5
	7	591.5	595.0

a. Test conditions as specified in the Optical Characteristics at 25°C section.

Packing Information

Products are packed in tubes as illustrate in Figure 15. Each tube contains a maximum of 10 units.

Figure 15: Packing Tube for HDSP-253x

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