High Efficiency 1.5MHz 1A Synchronous Step Down Converter

1 Features

- 4.5V to 100V Wide Operational Range
- Continuous Output Current: 1A
- Integrated 500mΩ/200mΩ Low On-Resistance Power MOS
- Constant-On-Time Control
- Low Quiescent Current: 220μA
- Low Shutdown Current: 4μA
- Programmable Switching Frequency from 300kHz to 800kHz
- Selectable FPWM/PFM Mode
- Support Isolated-Buck Topology in FCCM
- Built-in Pull-up Current at EN Pin
- Internal 2ms Soft Start function
- Integrated BST Charging Circuit
- Low Drop Out Mode Support 97% Duty Cycle
- Pre-bias Start-up
- Available in ESOP8 package

2 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications

3 Description

The GD30DC1901 is a 100V, 1A synchronous step-down converter featuring integrated high-side and low-side MOSFETs. Utilizing advanced constant-on-time (COT) control, it offers a compact solution size with excellent load transient performance.

The integrated BST charging circuit reduces both cost and solution size. Its extended high-duty cycle makes it ideal for applications requiring a low drop-out feature. 220μA quiescent current saves the power, while its low off-current is particularly suitable for battery-powered applications.

The GD30DC1901 supports FCCM/PFM mode selection. FCCM mode ensures continuous conduction operation across all load ranges, enabling compatibility with isolated buck converter applications.

It includes built-in protection features such as cycle-by-cycle current limit, hiccup mode SCP, output over-voltage protection (OVP), feedback (FB) open protection, and thermal shutdown for excessive power dissipation.

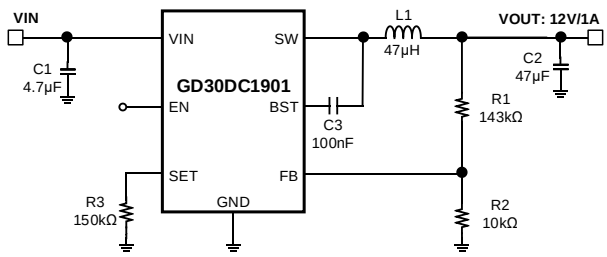
The GD30DC1901 is available in a compact ESOP8 package, making it a space-efficient solution.

Device Information[1]

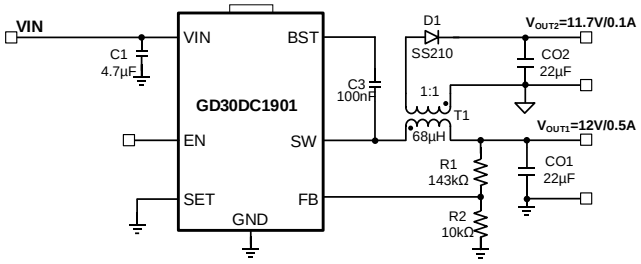
PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1901	ESOP8	4.90 mm x 3.90 mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



Buck Application



Isoated-Buck Application

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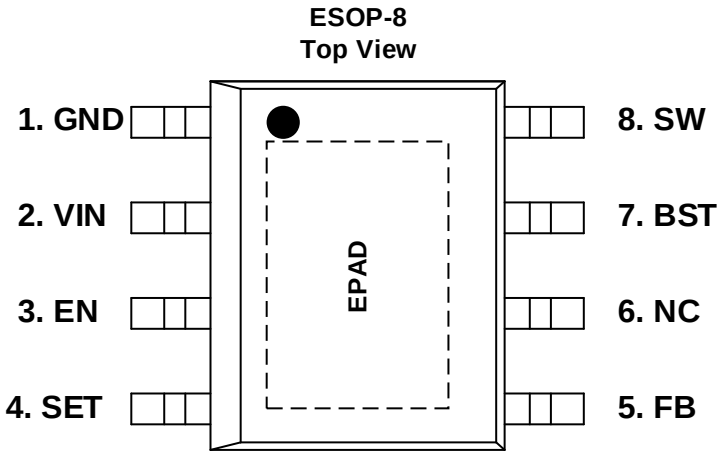
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	ESOP8		
GND	1	G	**Ground Pin.** Chip's GND connection. Connect to the ground of the system.
VIN	2	P	**Power supply**. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
EN	3	I	**Enable**. Pull high to enable the output. and pull low to disables the device and turns it into shutdown. Don't leave this pin floating.
SET	4	I	**Set Pin**. Frequency and Mode selection.
FB	5	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider from VOUT to GND.
NC	6		**No connection**. No connection pin for GD30DC1901.
BST	7	O	**Bootstrap**. Connect a high-quality BST capacitor between SW and BST to form a floating supply across the high-side switch driver.
SW	8	O	**Switch output**. Switching node of power stage. Connected to the internal MOSFET switches and inductor terminal.
EP	9	G	**Exposed Pad.** Connect the exposed pad to the PCB GND plane to ensure optimal thermal efficiency.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	−0.3		105	V
V_{SW}	Switching node voltage (SW)	−0.3(−5V in 10ns)		105	V
V_{BST}- V_{SW}	Bootstrap pin for high side power MOS driving.			6	V
I_{EN}	Max Input current into EN pin			100	μA
All other pins		−0.3		6	A
T_J	Operating junction temperature	−40		150	°C
T_{stg}	Storage temperature	−65		150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	4.5		100	V
V_{OUT}	Output voltage range	0.8		28	V
I_{OUT}	Output current	0		1	A
T_J	Operating junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	ESOP8	48	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	ESOP8	52	°C/W
$\Theta_{JC(BOT)}$	Junction to case (bottom) thermal resistance	ESOP8	2.3	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 60V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current	V_{FB}=0.82V		220		μA
I_{SHDN}	Shutdown current	EN = 0V		4		μA
V_{UVLO_RISE}	Vin Uvlo rising	V_{IN} rising	4.15	4.3	4.45	V
V_{UVLO_FALL}	Vin Uvlo falling	V_{IN} falling	3.85	4	4.15	V
V_{UVLO_HYS}	Vin Uvlo hysteresis			0.3		V
ENABLE						
V_{EN_RISE}	Rising enable threshold		1.1	1.2	1.3	V
V_{EN_FALL}	Falling enable threshold		0.9	1	1.1	V
$I_{EN\_PULL\_UP}$	EN pulled up current	EN=L		1		μA
		EN=H		4		
V_{EN_CLAMP}	EN clamp voltage	I_{EN}=100μA		6		V
VOLTAGE REFERENCE						
V_{FB}	V_{FB}		0.768	0.78	0.792	V
V_{FB_UV}	FB UVP threshold			140		mV
Soft Start						
T_{SS}	Soft-start time	V_{FB} from 10% to 90%		2		ms
Power Stage						
R_{HS_ON}	High side MOS ON resistance	V_{BST} – V_{SW} = 5V		500		mΩ
R_{LS_ON}	Low side MOS ON resistance			200		mΩ
LKG_{HS}	High-side leakage	V_{EN} = V_{SW} = 0V			1	μA
SWITCHING REGULATOR						
F_{SW}	FPWM Mode Switching frequency	SET = GND	240	300	380	KHz
		R_{SET} = 18.7K	400	500	600	
		R_{SET} = 37.4K	640	800	920	
	PFM Mode Switching frequency	R_{SET} = 75K	240	300	380	
		R_{SET} = 150K	400	500	600	
		SET Pin Float	640	800	920	
T_{ON_MIN}[1]	Min On time			150		nS
T_{ON_MAX}[1]	Max On time			0		uS
T_{OF_MIN}[1]	Min Off time			320		nS
CURRENT LIMIT						
I_{LIMIT_HS}[1]	High-side current limit		1.4	1.85	2.4	A
Over Temperature Protection						
T_{OTP}[1]	OTP threshold			140		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

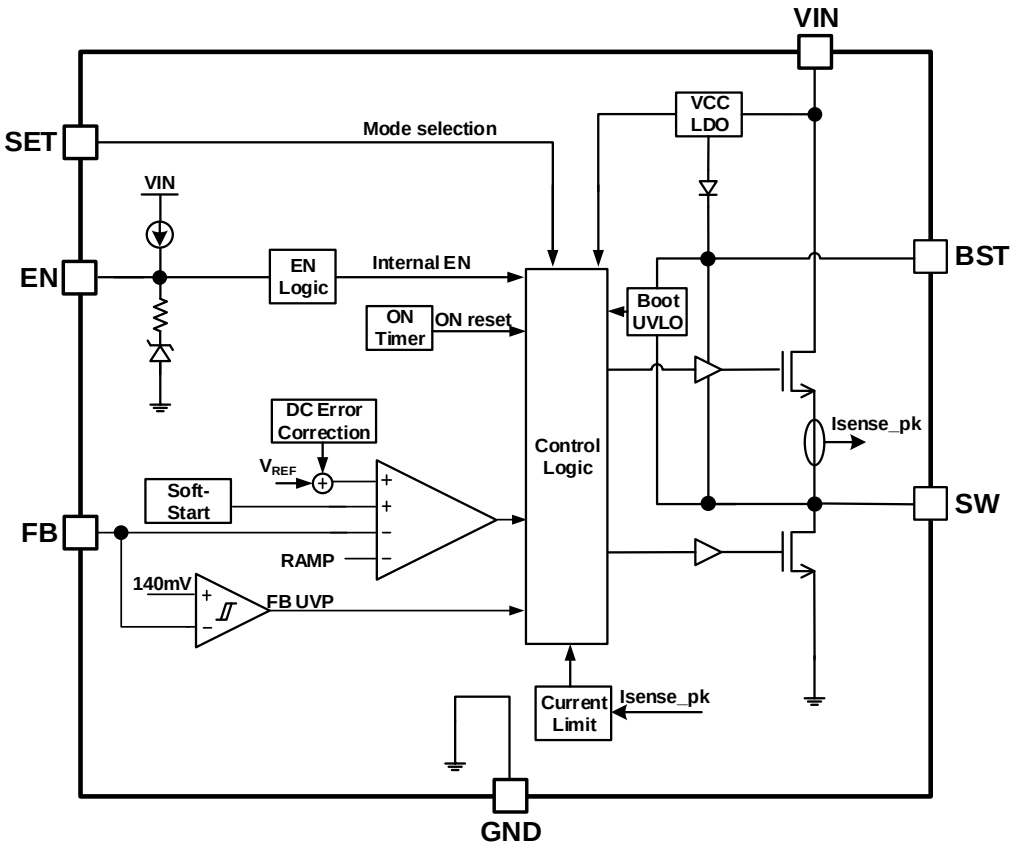


Figure 1. GD30DC1901 Functional Block Diagram

6.2 Operation

6.2.1 COT control loop operation

The GD30DC1901 is a fully integrated synchronous step-down switch-mode converter. It utilizes constant-on-time (COT) control to achieve fast transient response and simplify loop stabilization. At the start of each cycle, the high-side MOSFET (HS-FET) is activated when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), signaling that the output voltage is insufficient. The on-time duration is determined by both the input and output voltages, ensuring relatively stable switching frequency across the input voltage range.After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when VFB drops below VREF. Through this repetitive process, the converter regulates the output voltage.

The integrated low-side MOSFET (LS-FET) activates when the HS-FET is off, minimizing conduction losses. If both the HS-FET and LS-FET are simultaneously on, it creates a short circuit between the V_{IN} and GND, referred to as shoot-through. To prevent this, an internal dead time (DT) is employed between the transitions of HS-FET turning off and LS-FET turning on, or LS-FET turning off and HS-FET turning on.

In FPWM (Forced Pulse Width Modulation) mode, the LS-FET remains on continuously until the next HS-FET

pulse arrives. Conversely, in PFM (Pulse Frequency Modulation) mode, the LS-FET switches off when the inductor current drops to zero, causing the IC to enter a hi-z state until the next HS-FET pulse arrives. For detailed operational instructions, refer to the section below.

6.2.2 Light Load operation

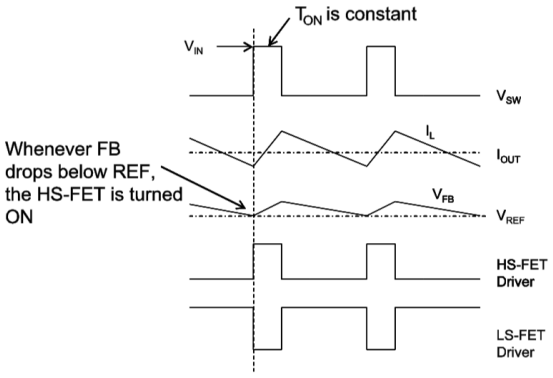


Figure 2. FPWM Operation

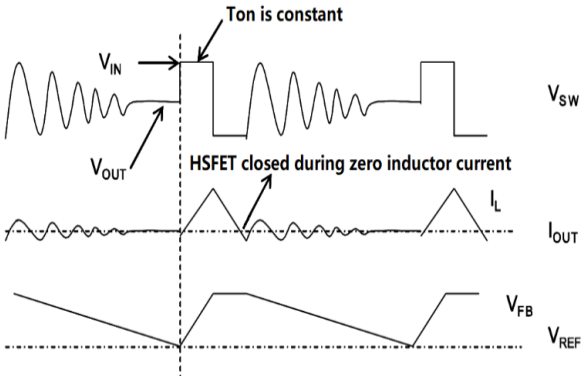


Figure 3. PFM Operation

The GD30DC1901 can be configured to work in either FPWM mode or PFM mode, as is shown in above Figure 2 and Figure 3.

In FPWM mode, the switching frequency remains stable as the load current varies. This helps reduce output voltage (V_{OUT}) ripple under light loads and simplifies the design of second-stage filters for damping power stage noise. However, because the internal power MOSFETs switch on and off more frequently, light-load efficiency is lower compared to PFM mode.

In PFM mode under light-load conditions, the V_{FB} cannot reach the V_{REF} while the inductor current approaches zero. The current modulator then takes over, keeping the inductor current near zero. During this time, the LS-FET driver enters a high-impedance (Hi-z) state, resulting in a slow output voltage drop. Consequently, the GD30DC1901 naturally reduces its switching frequency, achieving higher efficiency. However, as a trade-off, PFM mode experiences greater output voltage ripple.

For detailed setup methods regarding the operating mode and switching frequency of the GD30DC1901, refer to the section 6.2.7 Operation mode and frequency selection.

6.2.3 Heavy Load operation

For FPWM mode, the operating mechanism is the same as that in light load condition.

For PFM mode, As the output current rises from a light-load state, the regulation period of the current modulator becomes shorter. The HS-FET is activated more frequently, leading to an increase in the switching frequency. When the modulation time reduces to zero, the output current reaches the critical level. The critical output current can be calculated using the Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device switches to PWM mode once the output current surpasses the critical level. Afterward, the switching frequency remains relatively stable across the output current range.

6.2.4 Device Enable

The GD30DC1901 includes a dedicated enable control pin with positive logic. To activate the regulator, apply a voltage above 1.2V (typical) to the EN pin, and to disable it, set the EN pin voltage below 1V (typical). By using two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin. It recommend to use less than 30KΩ resistor for R_{ENDN}.

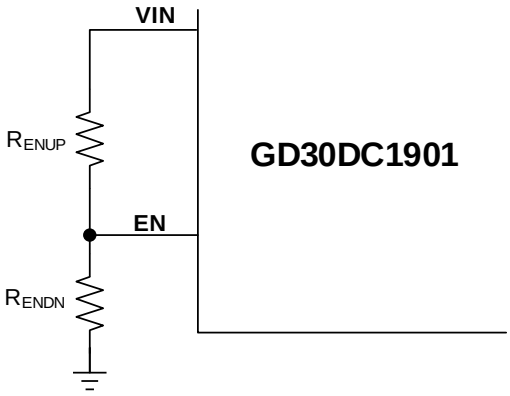


Figure 4. EN divider for adjustable UVLO

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 1 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (3)$$

6.2.5 Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) feature ensures the chip does not operate at inadequate supply voltages. The GD30DC1901 UVLO comparator monitors the input voltage, with a rising threshold of approximately 4.3V and a falling threshold of 4V.

6.2.6 Internal Soft Start (SS)

The soft-start (SS) function prevents output voltage overshoot during start-up. When the chip powers on, the internal circuit generates a soft-start voltage (V_{SS}) that gradually increases from 0V to 1V. While V_{SS} remains below V_{REF}, V_{SS} replaces V_{REF} as the reference for the error amplifier. Once V_{SS} surpasses V_{REF}, the error amplifier switches back to using V_{REF}. The soft-start duration is internally set to 2ms.

6.2.7 Operation mode and frequency selection

Table 1. Switching frequency set resistor selection

SET PIN	Operation Mode	Switching Frequency
SET Pin short to GND	FPWM	300kHz
R_{SET} = 18.7kΩ	FPWM	500kHz
R_{SET} = 37.4kΩ	FPWM	800kHz
R_{SET} = 75kΩ	PFM	300kHz
R_{SET} = 150kΩ	PFM	500kHz
SET Pin Float	PFM	800kHz

6.2.8 Isolated-buck application

The GD30DC1901 supports an isolated-buck topology to provide isolated V_{OUT}, requiring a transformer for operation. Energy transfer from the primary side to the secondary side occurs when the low-side synchronous switch of the buck converter is active. So it needs IC work in FPWM mode. For detailed information please refer to 7.1.1 *Isolated-Buck*.

6.2.9 Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The GD30DC1901 incorporates both peak current limit and valley current limit controls. During HS-FET operation, its current is monitored, and the HS-FET turns off upon reaching the peak current limit, enabling the LS-FET valley current limit control. The LS-FET remains active until its current falls below the valley limit. Once OCP occurs, the output voltage will drop down at the same time, which will cause VFB dropping down correspondingly, either 'VFB below FB UVP threshold(typically 140mV)' or 'OCP is occurred' happen, the device will start to timing typically 10ms deglitch time, if any of the above two conditions still exists, the device will enters GD30DC1901 will enter hiccup mode, until both of the conditions are removed, then the GD30DC1901 will back to normally switching again.

6.2.10 Thermal Shutdown

The GD30DC1901 includes thermal shutdown protection, with its junction temperature monitored internally. If the temperature exceeds the threshold (typically 140°C), the converter shuts down. This protection is non-latching, allowing the GD30DC1901 to automatically restart once the temperature decreases.

7 Application Information

7.1 Typical Application Circuits

7.1.1 Isolated-Buck

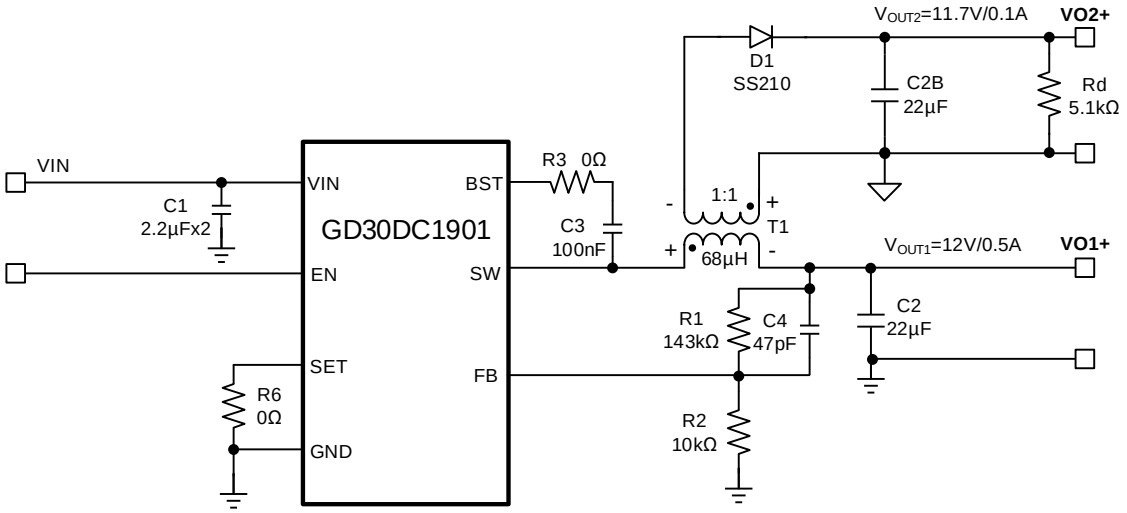


Figure 5. Isolated-buck application

An isolated Isolated-buck using the GD30DC1901 is shown Above. Inductor in a typical buck circuit is replaced with a coupled inductor (T1). A diode (D1) is used to rectify the voltage on a secondary output.

7.1.2 Buck

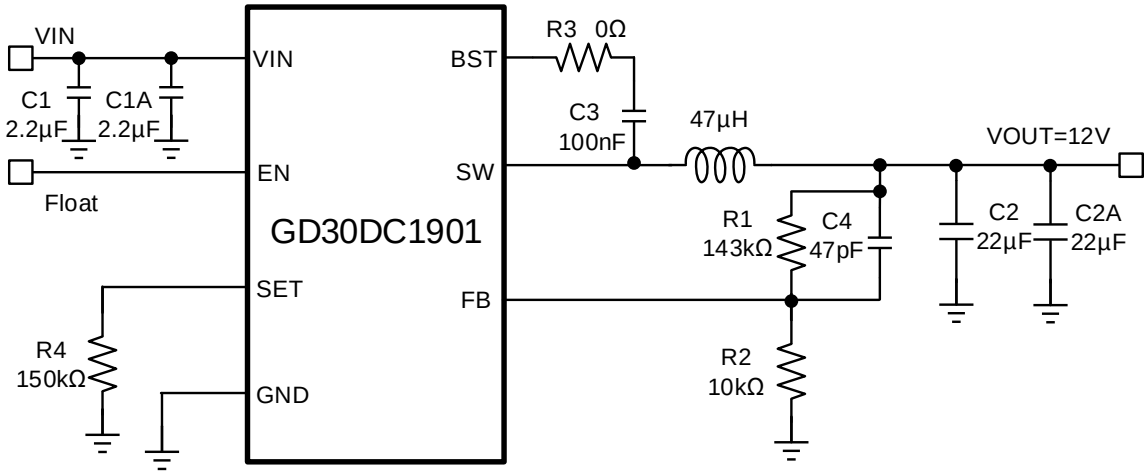


Figure 6. V_{IN}=48V, V_{OUT}=12V, I_{OUT}=1A, F_{SW}=500KHz, PFM MODE

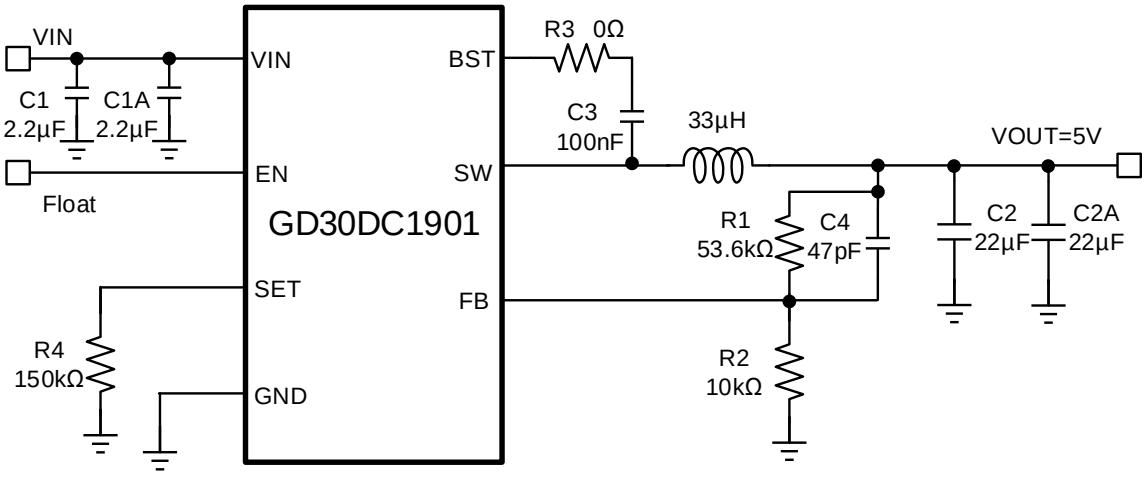


Figure 7. V_{IN}=48V, V_{OUT}=5V, I_{OUT}=1A, F_{SW}=500KHz, PFM MODE

7.2 Detailed Design Description

7.2.1 Setting the Output Voltage

The GD30DC1901 output voltage is configured via external resistor dividers, with a fixed reference voltage of 0.8V. The feedback network layout is shown in Figure 8.

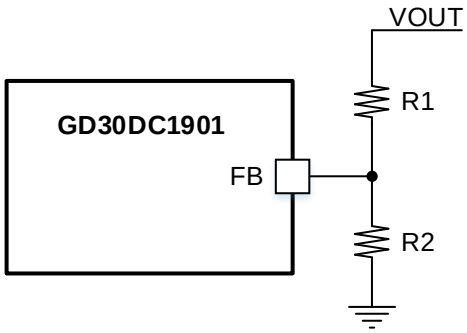


Figure 8. Feedback Network

Choose R1 and R2 using Equation(4):

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \quad (4)$$

7.2.2 Selecting the Inductor

An inductor is essential for providing continuous current to the load while being driven by the switched input voltage. A larger inductor minimizes ripple current and reduces output voltage ripple but comes with drawbacks such as a larger physical size, higher series resistance, and lower saturation current. For most designs, the suitable inductance value can be calculated using the following Equation(5):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (5)$$

Where ΔIL is the inductor ripple current.

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2. Resistor Selection for Common Output Voltages[1]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Cff (pF)	L (μH)	C_{OUT} (μF)
12	143	10	47	47	2*22
5	53.6	10	47	33	2*22

1. For a detailed design circuit, please refer to the Typical Application Circuits.

7.2.3 Selecting the Output Capacitor

The output capacitor is responsible for maintaining the DC output voltage ripple. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred for minimizing output voltage ripple, which can be estimated using the Equation(6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also influence the stability of the regulation system. The GD30DC1901 is designed to operate efficiently across a wide range of capacitance and ESR values.

7.2.4 Transformer Design rule

This topology requires a transformer, and energy transfer occurs from the primary to secondary side when the LS-FET of the GD30DC1901 is switched on. The key principles for transformer selection are as follows:

a) The saturation current on the primary side of T1 should exceed the peak current limit of GD30DC1901, which is typically 1.85A.

b) The selection of primary side inductance follows similar principles to a traditional COT buck converter.

c) T1's leakage inductance should not be too small, as it helps limit the secondary side current.

d) The turns ratio of the transformer should be designed considering the following:

The nominal voltage for the secondary output (V_{OUT2}) can be calculated using the Equation(7):

$$V_{OUT2} = \frac{(V_{OUT1} + V_F) \times N_S}{N_P} \quad (7)$$

Where V_F is the forward voltage drop of D1; N_P and N_S are the number of turns on the primary and secondary of T1.

The transformer turns ratio is determined by the ratio of the primary output voltage (V_{OUT1}) to the secondary output voltage (V_{OUT2}). In this design, the two outputs are nearly equal and a 1:1 turns ratio transformer is selected. Therefore, $N_P/N_S=1$.

For improved load regulation, adding a low-power LDO to the secondary output power loop is advised.

7.2.5 Primary Output Capacitor

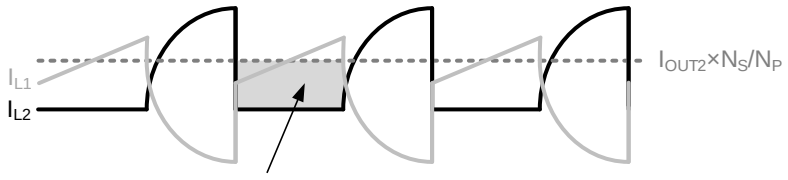


Figure 9. Current Waveforms for COUT$_1$ Ripple Calculation

The figure above illustrates the primary winding current waveform (I_{L1}) in an isolated buck converter. During the buck switch off-time, the reflected secondary winding current combines with the primary winding current. Consequently, the primary-side output voltage ripple differs from that of a traditional buck converter. If most of the load current is supplied by the secondary isolated output, the primary output voltage ripple can be approximated by the Equation(8):

$$\Delta V_{OUT1} = \frac{I_{OUT2} \times V_{OUT1} \times N_S}{f_{SW} \times C_{OUT1} \times V_{IN} \times N_P} \quad (8)$$

Where C_{OUT1} is primary side output capacitane, f_{SW} is the switching frequency of GD30DC1901. Select an appropriate primary-side output capacitance based on the voltage ripple requirements.

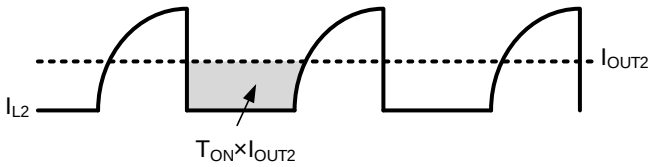


Figure 10. Secondary Current Waveforms for $COUT_2$ Ripple Calculation

Where C_{OUT2} is primary side output capacitane, f_{SW} is the switching frequency of GD30DC1901

Choose a suitable secondary-side output capacitance considering the voltage ripple requirements.

$$\Delta V_{OUT2} = \frac{I_{OUT2} \times V_{OUT1}}{f_{SW} \times C_{OUT2} \times V_{IN}} \quad (9)$$

7.2.6 Secondary Diode

The maximum reverse voltage across secondary-rectifier diode D1 $VD_{\_MAX}$ when the high-side buck switch is off can be calculated using Equation(10):

$$V_{D\_MAX} = \frac{N_S}{N_P} \times \left(V_{IN\_MAX} - V_{OUT1}\right) + V_{OUT2} \quad (10)$$

Where, V_{IN_MAX} is maximum input voltage, recommend to choose a secondary conducting diode whose voltage rating is larger than V_{D_MAX} and leave reasonable margin.

7.3 Typical Application Curves

V_{IN} = 48V, C_{IN} = 2x2.2uF,C_{OUT} = 2x22uF, T_A = 25°C, unless otherwise noted.

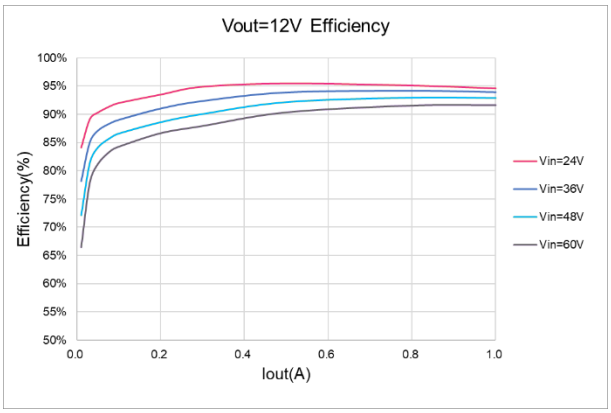


Figure 11. Efficiency vs. Output Current (F_{SW}=500kHz, PFM MODE, L=47μH)

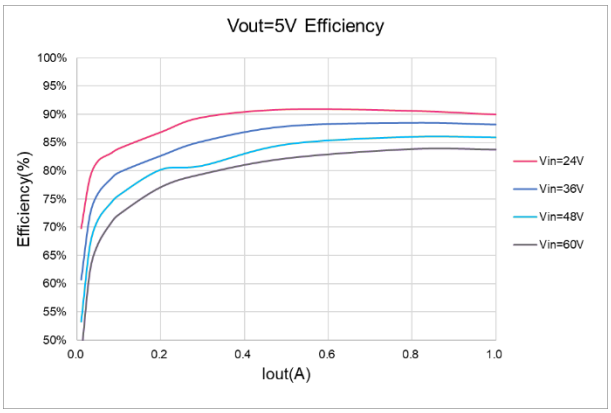


Figure 12. Efficiency vs. Output Current (F_{SW}=500kHz, PFM MODE, L=33μH)

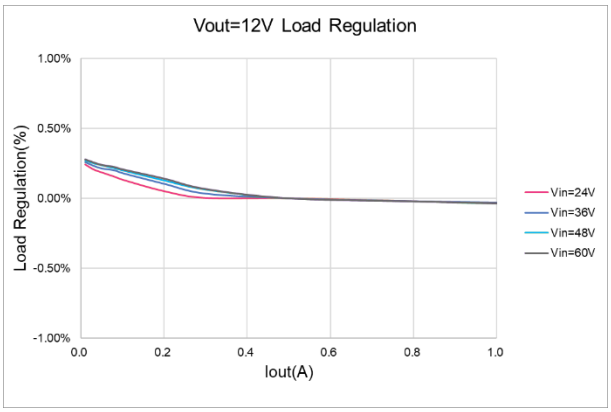


Figure 13. Load Regulation vs. Output Current (F_{SW}=500kHz , PFM MODE, L=47μH)

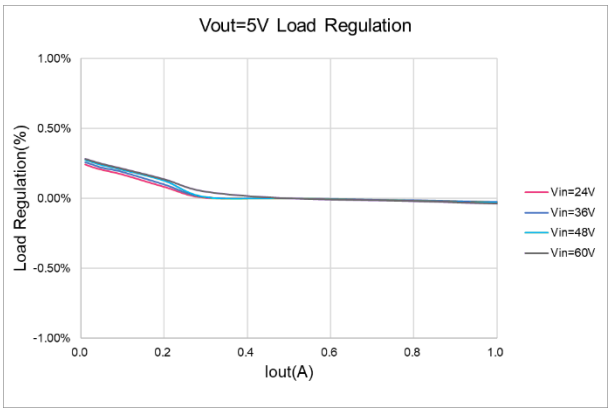


Figure 14. Load Regulation vs. Output Current (F_{SW}=500kHz , PFM MODE, L=33μH)

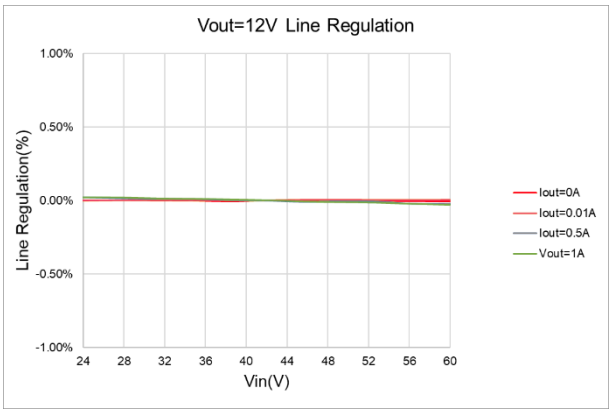


Figure 15. Line Regulation vs. Output Current (F_{SW}=500kHz , PFM MODE, L=47μH)

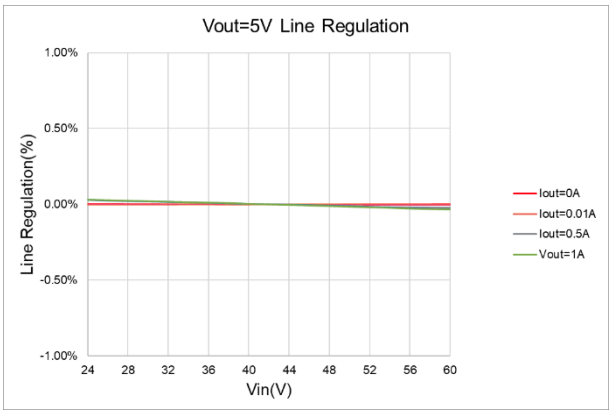


Figure 16. Load Regulation vs. Output Current (F_{SW}=500kHz , PFM MODE, L=33μH)

Typical Application Curves (continued)

V_{IN} = 48V, C_{IN} = 2x2.2uF,C_{OUT} = 2x22uF, T_A = 25°C, unless otherwise noted.

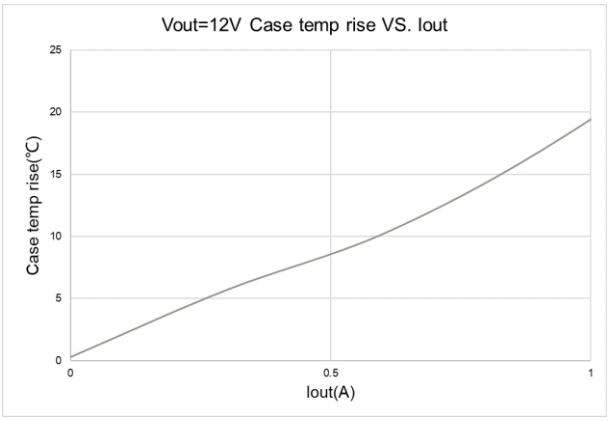


Figure 17. Thermal Rise vs. Output Current

(F_{SW}=500kHz , PFM MODE, L=47μH, no air flow)

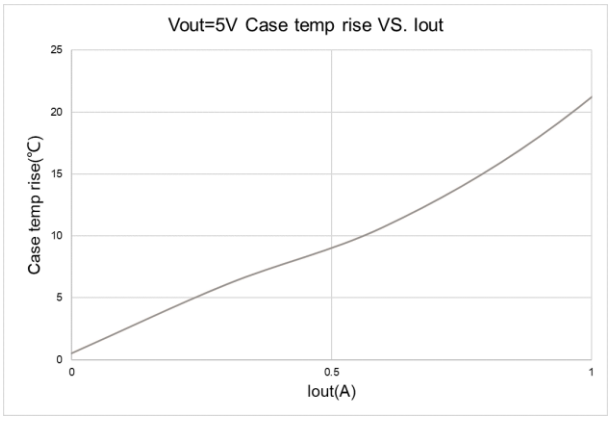


Figure 18. Thermal Rise vs. Output Current

(F_{SW}=500kHz , PFM MODE, L=33μH, no air flow)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2x2.2uF,C_{OUT} = 2x22uF, L1=47uH,TA = 25°C, unless otherwise noted.

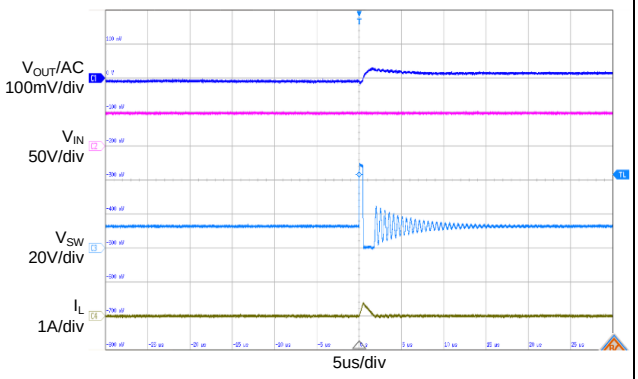


Figure 19. Output Ripple

(I_{OUT} = 0A, PFM MODE)

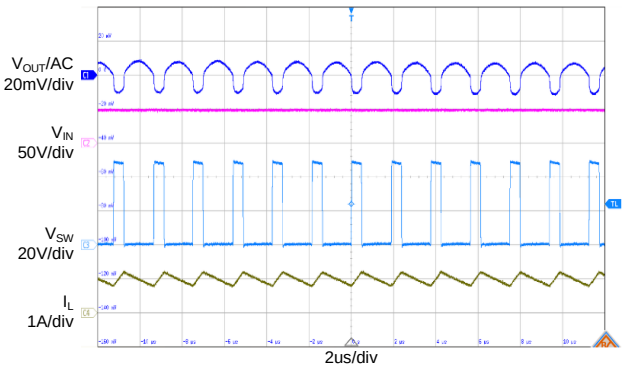


Figure 20. Output Ripple

(I_{OUT} = 1A)

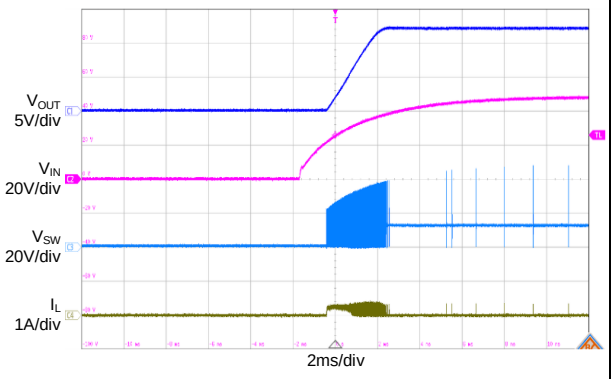


Figure 21. VIN StartUp without Load

(I_{OUT} = 0A, PFM MODE)

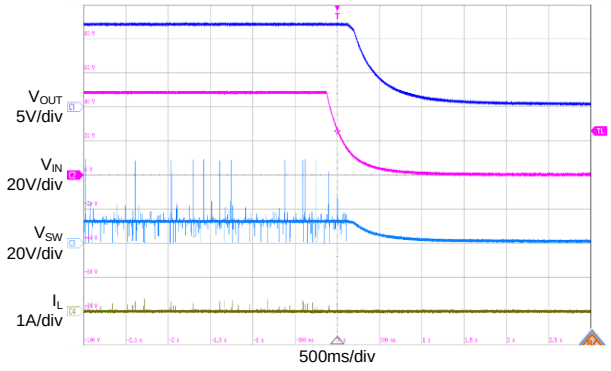


Figure 22. VIN ShutDown without Load

(I_{OUT} = 0A, PFM MODE)

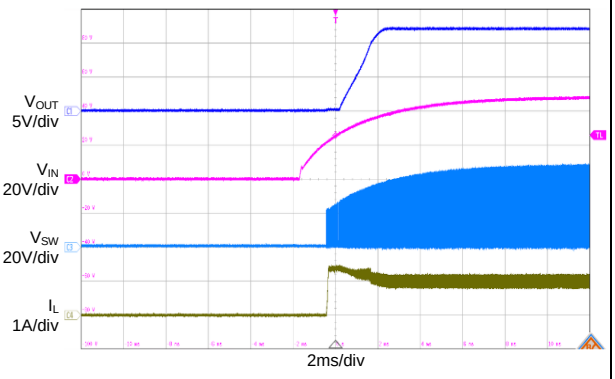


Figure 23. VIN StartUp with Load

(I_{OUT} = 1A)

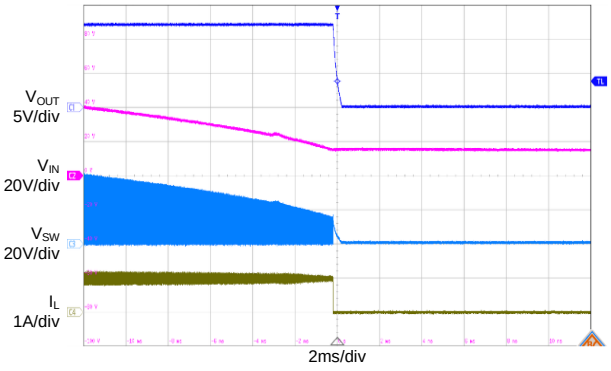


Figure 24. VIN ShutDown with Load

(I_{OUT} = 1A)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2x2.2uF,C_{OUT} = 2x22uF, L1=47uH,TA = 25°C, unless otherwise noted.

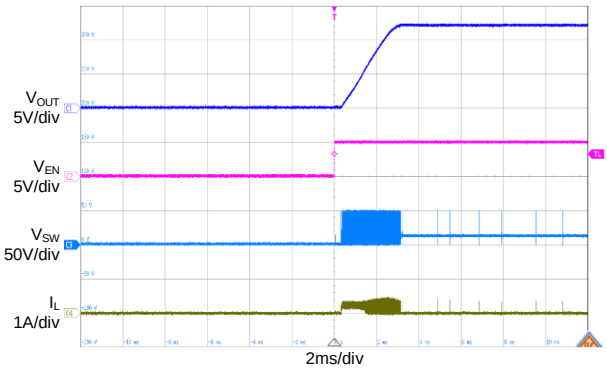


Figure 25. EN StartUp without Load

(I_{OUT} = 0A, PFM MODE)

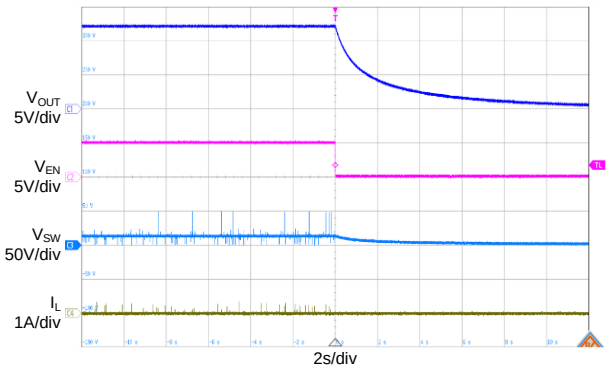


Figure 26. EN ShutDown without Load

(I_{OUT} = 0A, PFM MODE)

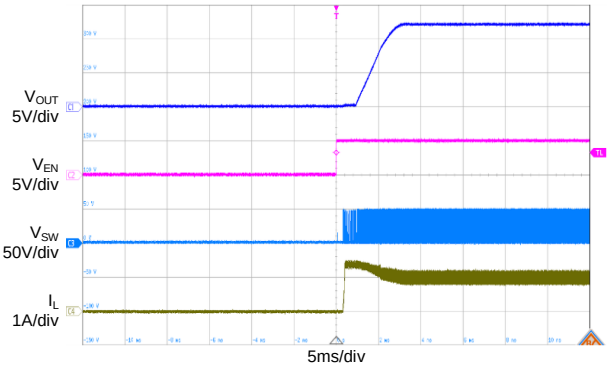


Figure 27. EN StartUp with Load

(I_{OUT} = 1A)

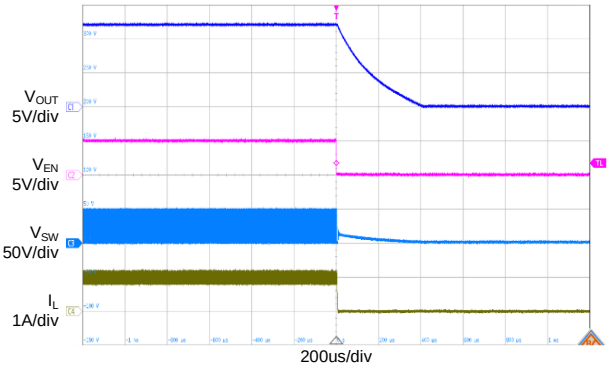


Figure 28. EN ShutDown with Load

(I_{OUT} = 1A)

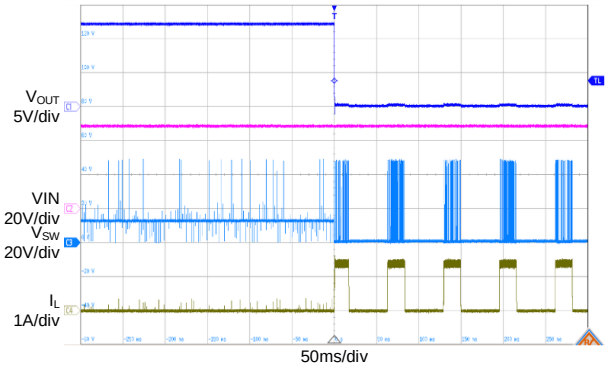


Figure 29. Short Circuit Entry

(I_{OUT} = 0A, PFM MODE)

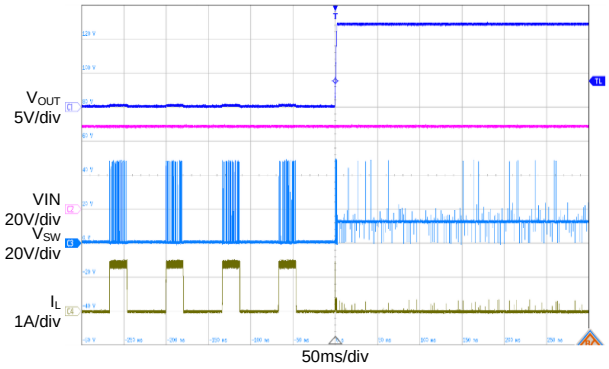


Figure 30. Short Circuit Recovery

(I_{OUT} = 0A, PFM MODE)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2x2.2uF,C_{OUT} = 2x22uF, L1=47uH,TA = 25°C, unless otherwise noted.

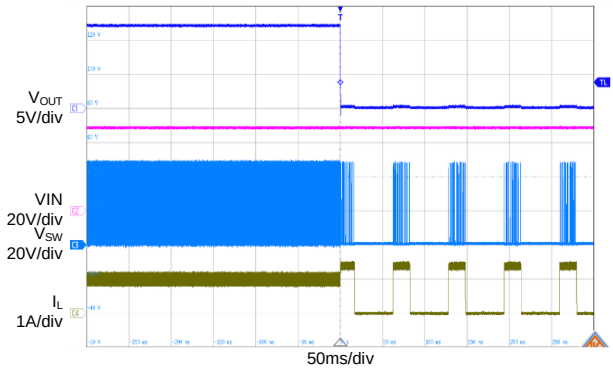


Figure 31. Short Circuit Entry

(I_{OUT} = 1A)

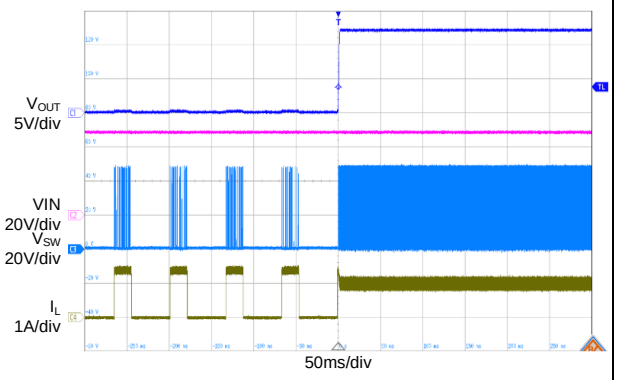


Figure 32. Short Circuit Recovery

(I_{OUT} = 1A)

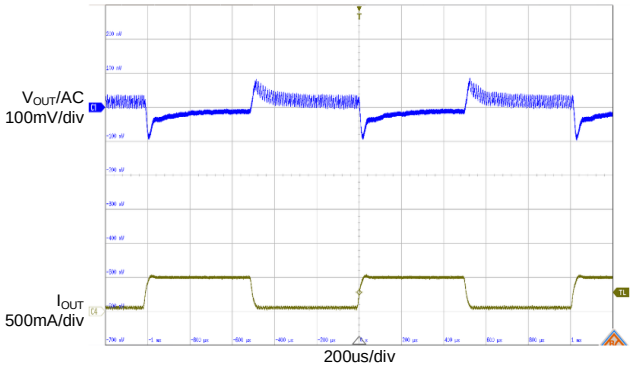


Figure 33. Load Traneient by E-load

(I_{OUT} = 0.05A to 0.5A, 3A/μs, PFM MODE)

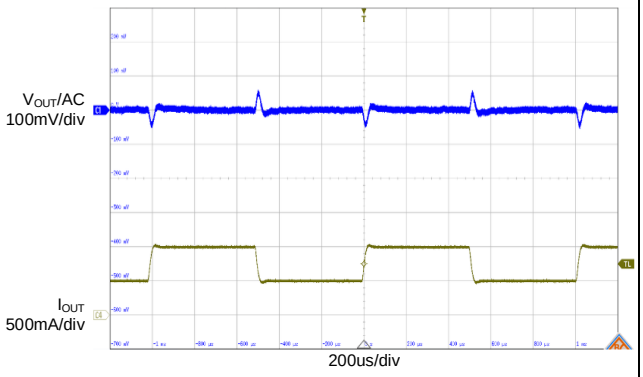


Figure 34. Load Traneient by E-load

(I_{OUT} = 0.5A to 1A, 3A/μs)

8 Layout Guidelines and Example

Proper layout design is essential for the stable operation of switching power supplies. In high-frequency switching converters, poor layout can lead to issues such as unstable operation and poor line or load regulation. For optimal performance, refer to the figure below and follow these guidelines:

1) Place the input capacitor as close to VIN and GND as possible.
2) Position external feedback resistors near the FB pin for best accuracy.
3) Keep the switching nodes (e.g., SW and BST) away from the feedback network to reduce interference. Ensure BST and SW trace as short as possible.
4) Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

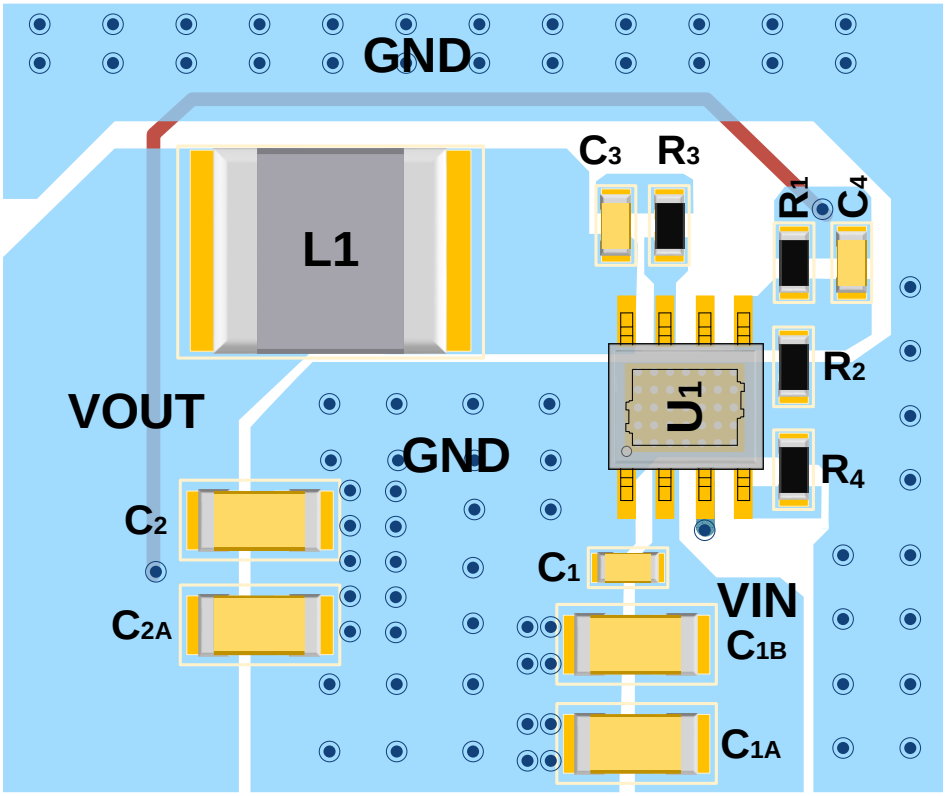
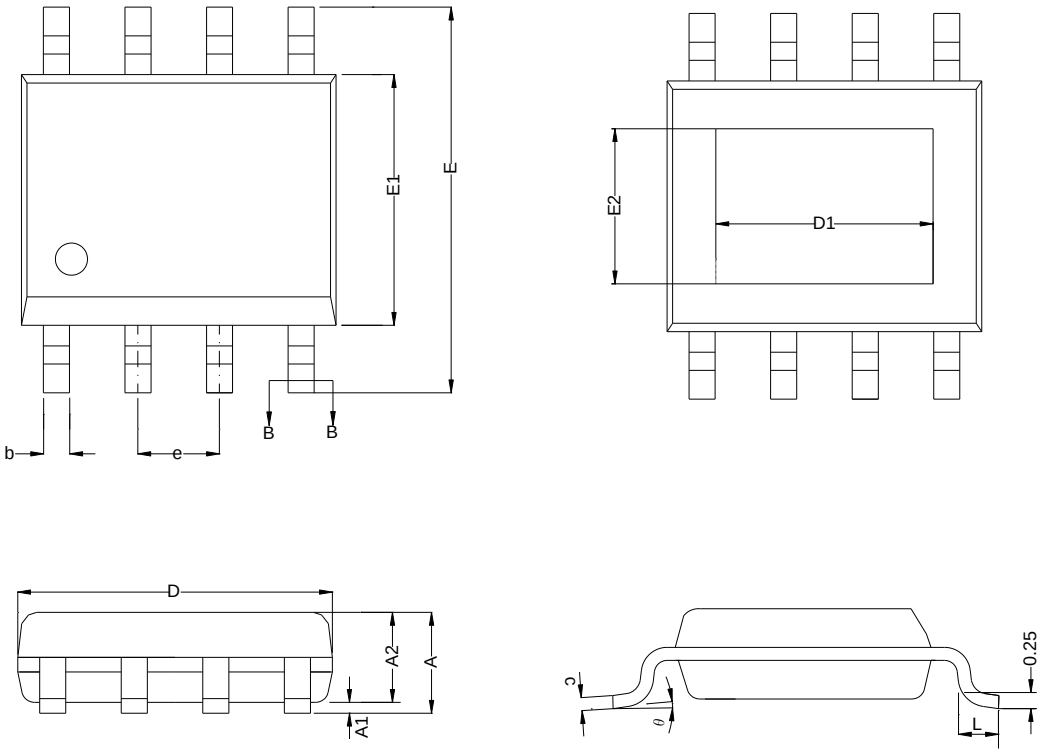


Figure 35. Typical GD30DC1901 Example Layout

9 Package Information

ESOP8 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *ESOP8 dimensions(mm)*.

Table 3. ESOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30		1.70
b	0.33		0.51
c	0.19		0.25
D	4.80	4.90	5.00
D1	3.15		3.45
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.26		2.56
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
IGD30DC1901WGTR-I	ESOP8	Green	Tape & Reel	4000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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