

150V Three Phase BLDC Gate Driver

1 Feature

- High-side floating bootstrap power supply design, withstand voltage of 150V
- Compatible with 5V, 3.3V input voltage V_{HINx}/V_{LINx}
- Maximum frequency support up to 500KHz
- · Built-in dead time control circuit
- Under-voltage protection for upper and lower bridge power supplies, startup and protection points at 4.4V and 4.1V
- Internally integrated low-on-resistance bootstrap charging diode
- Output source/sink current lo+/lo- is +1.0A/-1.3A
- HIN input high-level active, controls upper bridge HO output
- LIN input high-level active, controls lower bridge LO output
- TSSOP20, QFN24 package
- RoHS compliant

2 Applications

- · Three-phase brushless DC motor driver
- · Electric vehicle controller

3 Description

The GD30DR1488 is a cost-effective dedicated three-phase BLDC gate driver circuit used for driving high-power MOSFET and IGBT gates. The IC integrates logic signal processing circuits, dead time control circuits, under-voltage protection circuits, level shifting circuits, pulse filtering circuits, and output driver circuits, specifically designed for use in the drive circuits of brushless motor controllers.

Device Information¹

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DR1488	TSSOP20	6.50mm x 4.40mm
GD30DK1400	QFN24	4.00mm x 4.00mm

1. For packaging details, see Package Information section.

Simplified Application Schematic

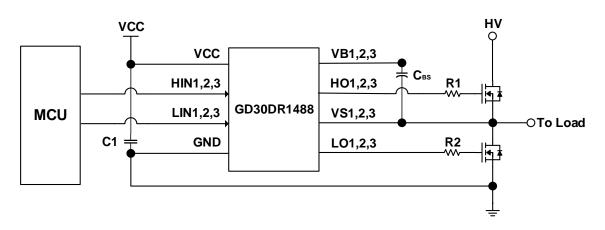




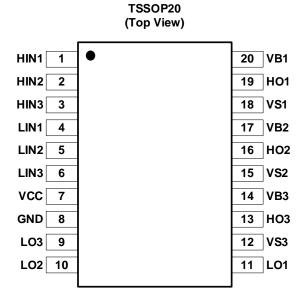
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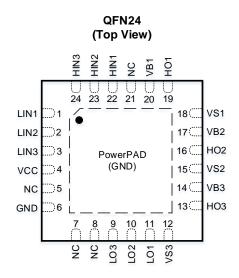
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4 Device Overview

4.1 Pinout and Pin Assignment





4.2 Pin Description

F	Pin sequenc	е	DIN TYPE	FUNCTION	
PIN	ESOP8	QFN24	PIN TYPE	FUNCTION	
HIN1	1	22	I	Upper bridge gate drive control logic signal input 1	
HIN2	2	23	I	Upper bridge gate drive control logic signal input 2	
HIN3	3	24	I	Upper bridge gate drive control logic signal input 3	
LIN1	4	1	I	Lower bridge gate drive control logic signal input 1	
LIN2	5	2	I	Lower bridge gate drive control logic signal input 2	
LIN3	6	3	I	Lower bridge gate drive control logic signal input 3	
VCC	7	4	Р	Gate driver power supply input pin, connect a 10µF or larger X5R or	
VCC	,	4	Г	X7R ceramic capacitor between VCC and GND	
GND	8	6	G	Ground	
LO3	9	9	0	Lower bridge gate drive control logic signal output 3	
LO2	10	10	0	Lower bridge gate drive control logic signal output 2	
LO1	11	11	0	Lower bridge gate drive control logic signal output 1	
VS3	12	12	I	Upper bridge floating ground 3	
HO3	13	13	0	Upper bridge gate drive control logic signal output 3	
VB3	14	14	0	Upper bridge bootstrap power supply 3, bootstrap capacitor	
V D3	14	14	J	connected between VB3 and VS3	
VS2	15	15	I	Upper bridge floating ground 2	
HO2	16	16	0	Upper bridge gate drive control logic signal output 2	



F	Pin sequenc	е	PIN TYPE	FUNCTION
PIN	ESOP8	QFN24	PINITPE	FUNCTION
VB2	17	17	0	Upper bridge bootstrap power supply 2, bootstrap capacitor connected between VB2 and VS2
VS1	18	18	1	Upper bridge floating ground 1
HO1	19	19	0	Upper bridge gate drive control logic signal output 1
VB1	20	20	0	Upper bridge bootstrap power supply 1, bootstrap capacitor connected between VB1 and VS1
NC		5, 7, 8, 21		No connection

^{1.} I = Input, O = Output, P = Power, G = Ground.



5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)1

SYMBOL	PARAMETER	MIN	MAX	UNIT
VB1,2,3	Upper bridge bootstrap power supply	-0.3	150	٧
VS1,2,3	Upper bridge floating terminal	VB-20	VB+0.3	٧
VHO1,2,3	Upper bridge output voltage	VS-0.3	VB+0.3	٧
VCC	Power supply	-0.3	20	V
VLO1,2,3	Lower bridge output voltage	-0.3	VCC+0.3	٧
PD	Maximum power consumption		500	mW
TJ	Operating junction temperature		150	°C
T _{stg}	Storage temperature		150	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL	PARAMETER		TYP	MAX	UNIT
VCC	Power supply	4	15	18	٧
1/64.2.2				150	V
VS1,2,3	Upper bridge floating terminal	-36 ²		150	V
VB1,2,3	Upper bridge bootstrap power supply		VS+15	VS+18	V
CL	Upper and lower bridge load capacitance			22	nF
VIN	Upper and lower bridge input level		3.3	5.0	V
TA	Operating ambient temperature	-40		125	°C

^{1.} Direct current negative voltage, at this time the minimum value of VB-VS is 12V.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
Vesd(HBM)	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017 ¹	±2000	V
V _{ESD(CDM)}	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022 ²	±200	V

^{1.} JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

^{2.} Instantaneous negative voltage with a width of 100ns.

^{2.} JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



5.4 Thermal Resistance

SYMBOL 1	CONDITIONS	TSSOP20	QFN24	UNIT
ΘЈА	Natural convection, 2S2P PCB	100	49	°C/W

^{1.} Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

 V_{CC} = 15V, VB1,2,3 = 15V, VS1,2,3 = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PA	RAMETER					
VIH1,2,3	High level at the input		2.5			V
VIL1,2,3	Low level at the input				0.8	V
VHOH1,2,3	Upper bridge arm output high level	Difference with VB, lo+ = 10mA			100	mV
VHOL1,2,3	Upper bridge arm output low level	Difference with VB, Io- =				
V110L1,2,3	opper bridge arm output low level	10mA			50	mV
VI OH1 2.2	Lower bridge arm output high lovel	Difference with VCC, lo+ =			100	m)/
VLOH1,2,3	Lower bridge arm output high level	10mA			100	mV
VLOL1,2,3	Lower bridge arm output low level	Difference with GND, lo- =			50	mV
72021,2,0	25 No. 2 Nago ann capación los es	10mA				
IHINH		HIN1,2,3 = 5V		50		μΑ
IHINL	Input current	HIN1,2,3 = 0V		0		μΑ
ILINH	input ourient	LIN1,2,3 = 0V		0		μA
ILINL		LIN1,2,3 = 5V		50		μA
IO+	Output pull current	$Vo = 0V$, $V_{IN} = V_{IH}$, $PW \le$	1.0			Α
101	Output pull current	10µs		1.0		
IO-	Output sink current	Vo = 15V, V _{IN} = V _{IL} , PW≤ 10µs		1.3		Α
RBSD	Bootstrap diode charging resistor	VCC = 15V, VB = 0V		40		Ω
IQCC	Quiescent current	LIN1,2,3 = 0V		90		μΑ
IQCC	Quiescent current	LIN1,2,3 = 5V		250		μA
IODO4 0.0	Llanau bridera anno errica cont erromant	HIN1,2,3 = 0V		30		μA
IQBS1, 2,3	Upper bridge arm quiescent current	HIN1,2,3 = 5V		120		μΑ
VCCUV+	VCC undervoltage lockout voltage			4.4		V
VCCUV-	VCC undervoltage lockout voltage			4.1		V
VBSUV+	VB undervoltage lockout voltage			4.4		V
VBSUV-	VB undervollage lockout vollage			4.1		V
DYNAMIC	PARAMETER ¹					_
Switching	time characteristics of upper br	idge arm output HO				
ton	Rise delay			200		ns



Electrical Characteristics

 V_{CC} = 15V, VB1,2,3 = 15V, VS1,2,3 = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t _{off}	Fall delay				100		ns
t _r	Rise time				35		ns
t _f	Fall time				15		ns
Switching	time characteristics of lowe	er bri	dge arm output LO				
t _{on}	Rise delay				200		ns
t _{off}	Fall delay				100		ns
t _r	Rise time				35		ns
tf	Fall time				15		ns
Dead time	characteristic						
DT	Dead time				100		ns
МТ	Difference between rise and fall dead time				10		ns

^{1.} Dynamic electrical parameter CL=1000pF.



6 Functional Description

6.1 Block Diagram

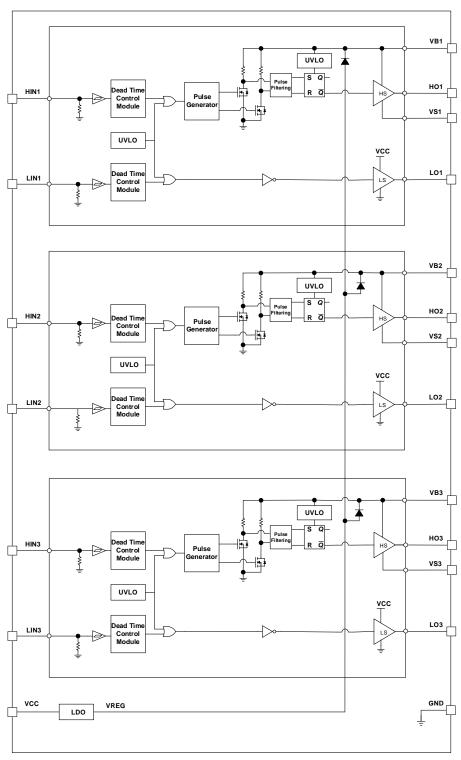
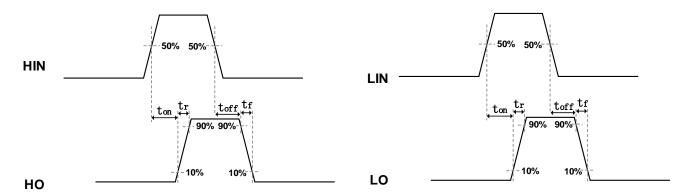


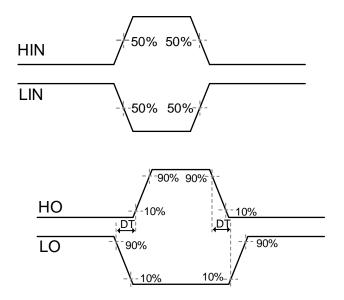
Figure 1. GD30DR1488 Functional Block Diagram



6.2 Switch Operation Waveform



6.3 Dead Time





6.4 Input-Output Logic Truth Table

Inj	out	Output		
HIN	LIN	НО	LO	
Low Level	Low Level	Low Level	Low Level	
Low Level	High Level	Low Level	High Level	
High Level	Low Level	High Level	Low Level	
High Level	High Level	Low Level	Low Level	



7 Application Information

The GD30DR1488 is widely used in three-phase brushless motor drive control. Section 7.1 briefly describes how to configure the application circuit for the GD30DR1488.

7.1 Typical Application Circuit

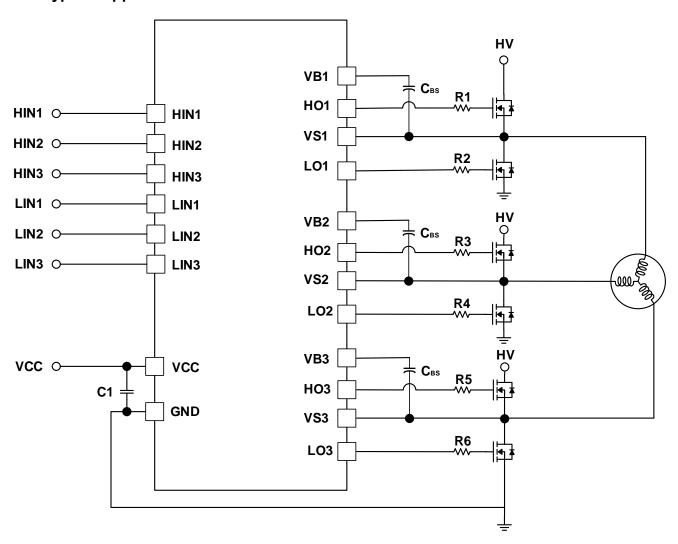
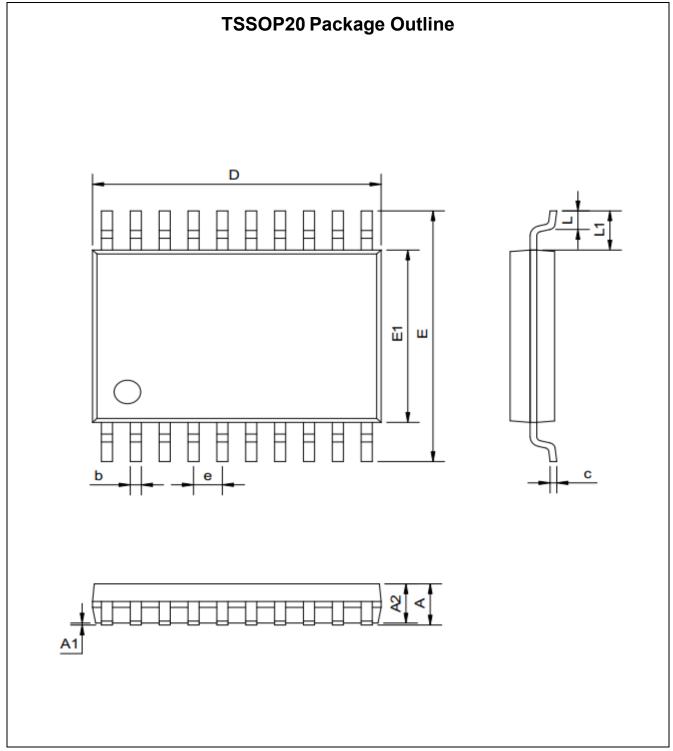


Figure 2. Brushless Motor Drive Reference Circuit



8 Package Information

8.1 Outline Dimensions



NOTES:

- 1. All dimensions are in millimeters.
- 2. Refer to the Table 1.TSSOP20 Dimensions (mm).

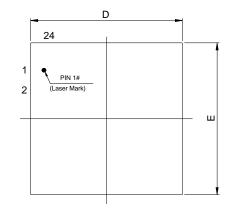


Table 1.TSSOP20 Dimensions (mm)

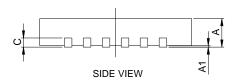
rabio irrecer to bimenerene (iiii)					
SYMBOL	MIN	MAX			
A		1.20			
A1	0.05	0.15			
A2	0.80	1.05			
b	0.19	0.30			
С	0.09	0.20			
D	6.40	6.60			
E	6.20	6.60			
E1	4.30	4.50			
е	0.65	BSC			
L	0.40	0.80			
L1	1.00	1.00 BSC			

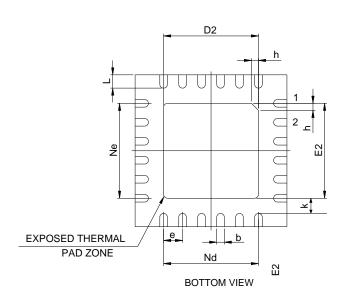


QFN24 Package Outline









NOTES:

1. Refer to the Table 2. QFN24 Dimensions (mm).



Table 2. QFN24 Dimensions (mm)

rabio 21 Qi 1424 Billionolollo (Illili)						
SYMBOL	MIN	MAX				
A	0.70/0.80	0.80/0.90				
A1		0.05				
b	0.20	0.30				
С	0.203	3 REF				
D	3.90	4.10				
D2	2.60	2.80				
е	0.50 BSC					
Nd	2.50 BSC					
Ne	2.50 BSC					
E	3.90	4.10				
E2	2.60	2.80				
L	0.35	0.45				
h	0.25	0.35				
К	0.25	REF				



9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DR1488FPTR-K	TSSOP20	Green	Tape & Reel	4000	–40°C to +125°C
GD30DR1488EUTR-K	QFN24	Green	Tape & Reel	5000	–40°C to +125°C



10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023
1.1	Add QFN24 thermal resistance parameters	2025



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