±250-mV or ±50-mV Input Isolated Delta-Sigma Modulators

Features

- CMTI: 100 kV/µs
- Input Voltage Range: ±250 mV or ±50 mV
- Very Low Offset Error: 150 µV or 50 µV at 25°C (Max)
- Very Low Gain Error:
  - 0.3% at 25°C (Max) for TPA8101
  - 0.3% at 25°C (Max) for TPA8102
- System-Level Diagnostic Features
- Wide Temperature Range: −40°C to +125°C
- TPA8101-SOAR-S is Qualified for Automotive Applications with the AEC-Q100 Reliability Test
- Finished Safety-Related Certifications:
  - CQC Certification per GB 4943.1
  - CB Certifications
  - 5000-V_{RMS} Isolation Rating per UL 1577
  - CSA, TUV Certifications
  - VDE Certification According to DIN VDE V 0884-17 (IEC60747-17)

Applications

- Industrial Automation
- Motor Control
- Power Supplies

Description

The device is a precision, delta-sigma modulator with an output separated from the input circuitry by a capacitive silicon dioxide insulation barrier. This barrier of the WSOP8 package is certified to provide isolation of up to 5000 V_{RMS} according to UL 1577.

The common-mode transient immunity (CMTI) of the device is significantly enhanced through innovative circuit design and optimized structure.

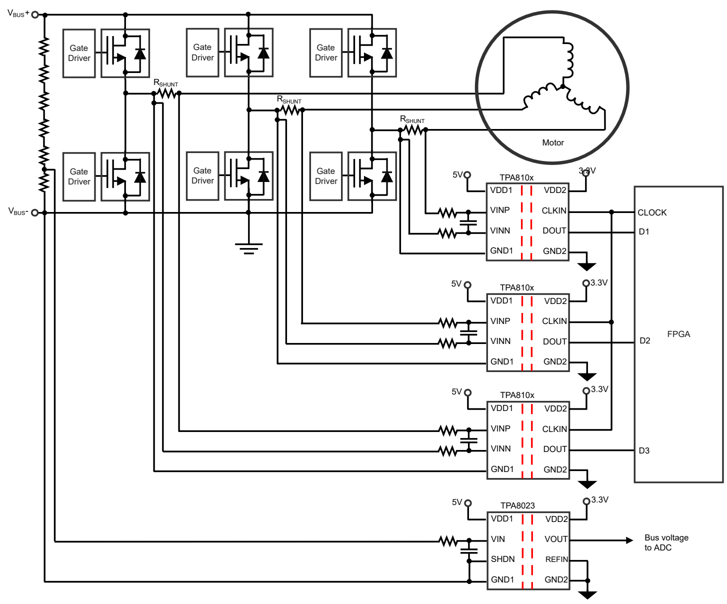
The input of the device is designed to connect to shunt resistors or other low-voltage level signal sources. The excellent performance of the device supports accurate current control in motor control applications. The common-mode overvoltage and missing high-side supply voltage detection feature system-level diagnostics.

The device is available in the WSOP8, WSOP16, and TSSOP8 packages, and is characterized from −40°C to +125°C.

Quick Selection Guide:

Product	Input Range	Clock Type
TPA8101	±250 mV	Clock In
TPA8102	±50 mV	Clock In

Typical Application Circuit



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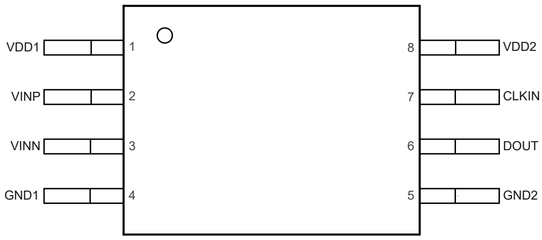
Revision History

Date	Revision	Notes
2023-09-29	Rev.A.0	Initial version.
2024-12-18	Rev.A.1	Added new part numbers: TPA8101-SOBR and TPA8101-SOAR-S. Updated Safety-Related certificates number. Updated the Order Information. Updated the Tape and Reel Information.
2025-06-09	Rev.A.2	Added new part number: TPA8102-SOAR and related specifications. Added Sinc^3 filter test conditions of Typical Perfomance Characteristics. Added quick selection guide. Updated the POD format of the WSOP8. Updated the Insulation Specifications of TSSOP8 package. Changed the Maximum Gain Error specification of TPA8102 from "±0.15%" to "±0.3%. Updated the AC PSRR, THD, SNR, SINAD and SFDR specifications of TPA8102.
2025-09-03	Rev.A.3	Added the digital interface timing of TPA8101 and TPA8102. Changed the Maximum Gain Error specification of the TPA8101 from "±0.15%" to "±0.3%. Updated the status of the VDE certificate. The actual product remains unchanged.

Pin Configuration and Functions

TPA810x
WSOP8
Top View



TPA810x
TSSOP8
Top View

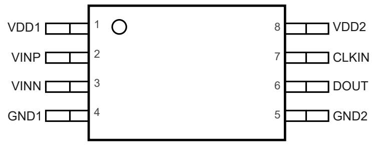


Table 1. Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD1		High-side power supply.
2	VINP	I	Positive analog input.
3	VINN	I	Negative analog input.
4	GND1		High-side analog ground.
5	GND2		Low-side analog ground.
6	DOUT	O	Modulator data output.
7	CLKIN	I	Modulator clock input.
8	VDD2		Low-side power supply.

TPA810x
WSOP16
Top View

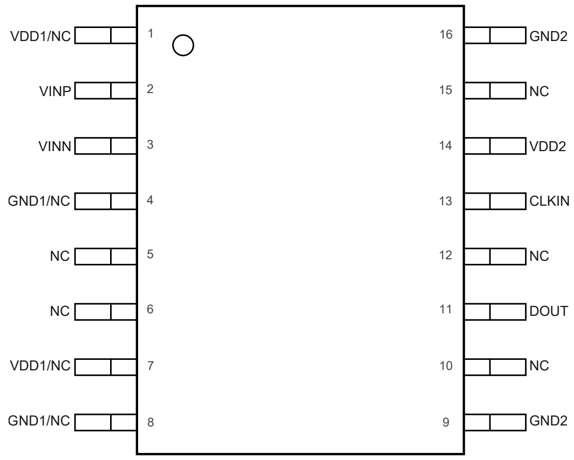


Table 2. Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD1/NC		One of the Pin1 or Pin7 needs to be connected to the high-side power supply, and the other pin can be connected to the high-side power supply or left float.
2	VINP	I	Positive analog input.
3	VINN	I	Negative analog input.
4	GND1/NC		One of the Pin4 or Pin8 needs to be connected to the high-side analog ground, and the other pin can be connected to the high-side analog ground or left float.
5	NC		Not connect.
6	NC		Not connect.
7	VDD1/NC		One of the Pin1 or Pin7 needs to be connected to the high-side power supply, and the other pin can be connected to the high-side power supply or left float.
8	GND1/NC		One of the Pin4 or Pin8 needs to be connected to the high-side analog ground, and the other pin can be connected to the high-side analog ground or left float.
9	GND2		Low-side analog ground.
10	NC		Not connect.
11	DOUT	O	Modulator data output.
12	NC		Not connect.
13	CLKIN	I	Modulator clock input.
14	VDD2		Low-side power supply.
15	NC		Not connect.
16	GND2		Low-side analog ground.

Specifications

Absolute Maximum Ratings (1)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage, VDD1 to GND1 or VDD2 to GND2	−0.3	7	V
V_{INPUT}	Analog Input Voltage at VINP, VINN	GND1 – 6	VDD1 + 0.5	V
	Digital Input or Output Voltage at CLKIN, DOUT	GND1 – 0.5	VDD2 + 0.5	V
I_{IN}	Input Current to Any Pin except Supply Pins	−10	10	mA
T_J	Operating Virtual Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{DD1}	High-Side Supply Voltage (VDD1 to GND1)	3.0	5.0	5.5	V
V_{DD2}	Low-Side Supply Voltage (VDD2 to GND2)	3.0	3.3	5.5	V
T_A	Operating Ambient Temperature	−40	25	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
WSOP8	85	43	°C/W
TSSOP8	191	44	°C/W
WSOP16	83	41	°C/W

Insulation Specifications

The value of UL and VDE is provided by lab test, and the UL and VDE certifications are ongoing.

Parameter		Conditions	Value		Unit
			WSOP8	TSSOP8	
CLR	External Clearance	Shortest terminal-to-terminal distance through air	8.0	4.0	mm
CPG	External Creepage	Shortest terminal-to-terminal distance across the package surface	8.0	4.0	mm
DTI	Distance through the Insulation	Minimum internal gap (internal clearance)	22	22	μm
DTC	Distance through the Molding Compound	Minimum internal distance across the conductors inside the package	0.8	0.8	mm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	> 600	> 600	V
	Material Group	According to IEC 60664-1	I	I	
	Over-Voltage Category	For Rated Mains Voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		For Rated Mains Voltage ≤ 300 V_{RMS}	I-IV	I-III	
		For Rated Mains Voltage ≤ 600 V_{RMS}	I-IV	I-II	
		For Rated Mains Voltage ≤ 1000 V_{RMS}	I-III	I-I	
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
DIN V VDE V 0884-17 (1)(2)					
V_{IORM}	Maximum Repetitive Isolation Voltage	AC voltage	1700	700	V_{PK}
V_{IOWM}	Maximum Working Isolation Voltage	AC voltage; TDDB test	1200	500	V_{RMS}
		DC voltage	1700	700	V_{DC}
V_{IOTM}	Maximum Transient Isolation Voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7000	5300	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage (3)	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	6500	5000	V_{PK}
q_{pd}	Apparent Charge	Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	≤ 5	
		Method b1; at routine test (100% production) and preconditioning (type	≤ 5	≤ 5	

Parameter		Conditions	Value		Unit
			WSOP8	TSSOP8	
		test), V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s			
C_{IO}	Isolation Capacitance	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation Resistance	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^9	> 10^9	Ω
UL 1577					
V_{ISO}	Withstanding Isolation Voltage	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	5000	3750	V_{RMS}

(1) All pins on each side of the barrier are tied together creating a two-terminal device.
(2) This coupler is suitable for safe electrical insulation only within the safety operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing must be carried out in oil.

Safety-Related Certifications

VDE	UL	TUV	CQC	CSA	CB
Certified according to DIN VDE V 0884-17	Certified according to UL 1577 and CSA Component Acceptance Notice 5A	Certified according to EN IEC 62368-1 and EN IEC 61010-1	Certified according to GB 4943.1	Certified CSA C22.2 No. 62368-1 and CAN/CSA-C22.2 No. 60601-1	Certified according to EN IEC 62368-1
Certificate No. 40054570	Report Reference E524241	Registration No. AK506327310001	Certificate No. CQC23001393276	Certificate No. UL-CA-2336696-1	Ref. Certif. No. CN59992

Safety Limiting Values

Parameter	Conditions (1)	Min	Typ	Max	Unit
Safety Input, Output or Supply Current	$R_{θJA}$ = 85°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C, WSOP8 package			267	mA
	$R_{θJA}$ = 191°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C, TSSOP8 package			119	mA
	$R_{θJA}$ = 85°C/W, VDD1 = VDD2 = 3.6 V, T_J = 150°C, T_A = 25°C, WSOP8 package			408	mA
	$R_{θJA}$ = 191°C/W, VDD1 = VDD2 = 3.6 V, T_J = 150°C, T_A = 25°C, TSSOP8 package			182	mA
Safety Total Power	$R_{θJA}$ = 85°C/W, T_J = 150°C, T_A = 25°C, WSOP8 package			1470	mW
	$R_{θJA}$ = 191°C/W, T_J = 150°C, T_A = 25°C, TSSOP8 package			655	mW
Maximum Safety Temperature				150	°C

(1) The assumed junction-to-air thermal resistance in the Thermal Information is that of a device installed on a high-K test board for leaded surface-mount packages.

Electrical Characteristics—TPA8101

All test conditions: minimum and maximum specifications are at T_A = −40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VINP = –250 mV to +250 mV, and VINN = 0 V; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog Input						
$V_{Clipping}$	Differential Input Voltage before Clipping Output	VINP – VINN		±320		mV
V_{FSR}	Specified Linear Differential Full-Scale	VINP – VINN	–250		250	mV
V_{CM}	Specified Common-Mode Input Voltage	(VINP + VINN) / 2 to GND1	–0.16		VDD1 – 2.5	V
	Absolute Common-Mode Input Voltage (1)	(VINN + VINP) / 2 to GND1	–2		VDD1	V
V_{CMov}	Common-Mode Overvoltage Detection Level		VDD1 – 2.4			V
CMRR	Common-Mode Rejection Ratio	f_{IN} = 0 Hz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		–95		dB
		f_{IN} = 10 kHz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		–100		
C_{IND}	Differential Input Capacitance			1		pF
R_{IN}	Single-Ended Input Resistance	VINN = GND1		19		kΩ
R_{IND}	Differential Input Resistance			22		kΩ
I_{IB}	Input Bias Current	VINP = VINN = GND1, I_{IB} = (I_{IBP} + I_{IBN}) / 2	–22	–17		μA
TCI_{IB}	Input Bias Current Drift			1		nA/°C
BW_{IN}	Input Bandwidth			1.2		MHz
DC Accuracy						
DNL	Differential Nonlinearity (1)	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral Nonlinearity (1)	Resolution: 16 bits	–4	±1	4	LSB
E_O	Offset Error	VDD1 = 5 V, T_A = 25°C, VINP = VINN = GND1	–150	±5	150	μV
TCE_O	Offset Error Thermal Drift (1)		–1	±0.15	1	μV/°C
E_G	Gain Error	at 25°C	–0.3	±0.005	0.3	%
TCE_G	Gain Error Thermal Drift (1)		–40	±20	40	ppm/°C
PSRR	Power-Supply Rejection Ratio	VINP = VINN = GND1, 3.0 V ≤ VDD1 ≤ 5.5 V, at DC		90		dB
		VINP = VINN = GND1, VDD1 = 5 V, 10 kHz, 100-mV ripple		80		dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AC Accuracy						
SNR	Signal-to-Noise Ratio	f_{IN} = 1 kHz		86		dB
SINAD	Signal-to-Noise + Distortion	f_{IN} = 1 kHz		85		dB
THD	Total Harmonic Distortion	VDD1 = 5.0 V, 5 MHz ≤ f_{CLKIN} ≤ 20 MHz, f_{IN} = 1 kHz		–82		dB
		VDD1 = 3.3 V, 5 MHz ≤ f_{CLKIN} ≤ 20 MHz, f_{IN} = 1 kHz		–80		dB
SFDR	Spurious-Free Dynamic Range	f_{IN} = 1 kHz		84		dB
Digital Inputs/Outputs						
I_{IN}	Input Current (1)	GND2 ≤ V_{IN} ≤ VDD2			7	µA
C_{IN}	Input Capacitance			4		pF
V_{IH}	High-Level Input Voltage (1)		0.7 × VDD2			V
V_{IL}	Low-Level Input Voltage (1)				0.3 × VDD2	V
C_{LOAD}	Output Load Capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	High-Level Output Voltage	I_{OH} = –20 µA	VDD2 – 0.1			V
		I_{OH} = –4 mA	VDD2 – 0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	V
Power Supply						
$VDD1_{UV}$	Undervoltage Detection Threshold Voltage of VDD1	VDD1 falling		2.1	2.4	V
I_{DD1}	High-Side Supply Current	3.0 V ≤ VDD1 ≤ 5.5 V		13	18	mA
I_{DD2}	Low-Side Supply Current	3.0 V ≤ VDD2 ≤ 5.5V		4	8	mA
Switching Characteristics (1)						
f_{CLKIN}	CLKIN Clock Frequency	4.5 V ≤ VDD2 ≤ 5.5 V	5		21	MHz
		3.0 V ≤ VDD2 ≤ 5.5 V	5		20	
t_{CLKIN}	CLKIN Clock Period	4.5 V ≤ VDD2 ≤ 5.5 V	47.6		200	ns
		3.0 V ≤ VDD2 ≤ 5.5 V	50		200	
t_{HIGH}	CLKIN Clock High Time		20	25	120	ns
t_{LOW}	CLKIN Clock Low Time		20	25	120	ns
t_H	DOUT Hold Time after Rising Edge of CLKIN	C_{LOAD} = 15 pF	3.1			ns
t_D	Rising Edge of CLKIN to DOUT Valid Delay	C_{LOAD} = 15 pF			15	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	DOUT Rise Time	10% to 90%, 2.7 V ≤ VDD2 ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3	ns
		10% to 90%, 4.5 V ≤ VDD2 ≤ 5.5 V, C_{LOAD} = 15 pF		0.8	3	
t_f	DOUT Fall Time	90% to 10%, 2.7 V ≤ VDD2 ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3	ns
		90% to 10%, 4.5 V ≤ VDD2 ≤ 5.5 V, C_{LOAD} = 15 pF		0.8	3	
t_{ISTART}	Interface Startup Time	VDD2 at 3 V (min) to DOUT valid with VDD1 ≥ 3 V		32		CLKIN Cycles
t_{ASTART}	Analog Startup Time	VDD1 step to 3.0 V with VDD2 ≥ 3 V, 0.1% settling		0.5		ms

(1) Provided by bench tests or design simulation.

Electrical Characteristics—TPA8102

Minimum and maximum specifications apply from T_A= −40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, VINP = –50 mV to +50 mV, and VINN = 0 V; typical specifications are at T_A= 25°C, VDD1 = 5 V, and VDD2 = 3.3 V, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Analog Input						
$V_{Clipping}$	Differential input voltage before clipping output	VINP – VINN		±64		mV
V_{FSR}	Specified linear differential full-scale	VINP – VINN	–50		50	mV
V_{CM}	Specified common-mode input voltage	(VINP + VINN) / 2 to GND1	–0.032		VDD1 – 2.5	V
	Absolute common-mode input voltage (1)	(VINN + VINP) / 2 to GND1	–2		VDD1	V
V_{CMov}	Common-mode overvoltage detection level		VDD1 – 2.4			V
CMRR	Common-mode rejection ratio	fIN = 0 Hz, VCM min ≤ VCM ≤ VCM max		–98		dB
		f_{IN}= 10 kHz, V_{CM}min ≤ V_{CM}≤ V_{CM}max		–98		
C_{IND}	Differential input capacitance			1		pF
R_{IN}	Single-ended input resistance	VINN = GND1		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IB}	Input bias current	VINP = VINN = GND1, I_{IB}= (I_{IBP} + I_{IBN}) / 2	–22	–17		μA
TCI_{IB}	Input bias current drift			1		nA/°C
BW_{IN}	Input bandwidth			1.2		MHz
DC Accuracy						
DNL	Differential nonlinearity(1)	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(1)	Resolution: 16 bits	–4	±1	4	LSB
E_O	Offset error	VDD1 = 5 V, T_A= 25°C, VINP = VINN = GND1	–50	±2.5	50	μV
TCE_O	Offset error thermal drift(1)		–1	±0.25	1	μV/°C
E_G	Gain error	at 25°C	–0.3	±0.01	0.3	%
TCE_G	Gain error thermal drift(1)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	VINP = VINN = GND1, 3.0 V ≤ VDD1 ≤ 5.5 V, at dc		108		dB
		VINP = VINN = GND1, VDD1 = 5 V, 10 kHz, 100-mV ripple		90		dB
AC Accuracy						

Parameter		Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	f_{IN}= 1 kHz		82.5		dB
SINAD	Signal-to-noise + distortion	f_{IN}= 1 kHz		82.3		dB
THD	Total harmonic distortion	VDD1 = 5.0 V, 5 MHz ≤ f_{CLKIN}≤ 20 MHz, f_{IN}= 1 kHz		–98		dB
		VDD1 = 3.3 V, 5 MHz ≤ f_{CLKIN}≤ 20 MHz, f_{IN}= 1 kHz		–93		dB
SFDR	Spurious-free dynamic range	f_{IN}= 1 kHz		100		dB
Digital Inputs/Outputs						
I_{IN}	Input current (1)	GND2 ≤ V_{IN}≤ VDD2			7	μA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage (1)		0.7 × VDD2			V
V_{IL}	Low-level input voltage (1)				0.3 × VDD2	V
CLOAD	Output load capacitance	f_{CLKIN}= 20 MHz		30		pF
VOH	High-level output voltage	I_{OH}= –20 μA	VDD2 – 0.1			V
		I_{OH}= –4 mA	VDD2 – 0.4			V
VOL	Low-level output voltage	I_{OL}= 20 μA			0.1	V
		I_{OL}= 4 mA			0.4	V
Power Supply						
$VDD1_{UV}$	undervoltage detection threshold voltage of VDD1	VDD1 falling		2.1	2.4	V
I_{DD1}	High-side supply current	3.0 V ≤ VDD1 ≤ 5.5 V		13	18	mA
I_{DD2}	Low-side supply current	3.0 V ≤ VDD2 ≤ 5.5V		4	8	mA
Switching Characteristics (1)						
f_{CLKIN}	CLKIN clock frequency	4.5 V ≤ VDD2 ≤ 5.5 V	5		21	MHz
		3.0 V ≤ VDD2 ≤ 5.5 V	5		20	
t_{CLKIN}	CLKIN clock period	4.5 V ≤ VDD2 ≤ 5.5 V	47.6		200	ns
		3.0 V ≤ VDD2 ≤ 5.5 V	50		200	
t_{HIGH}	CLKIN clock high time		20	25	120	ns
t_{LOW}	CLKIN clock low time		20	25	120	ns
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD}= 15 pF	3.1			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD}= 15 pF			15	ns

Parameter		Conditions	Min	Typ	Max	Unit
t_r	DOUT rise time	10% to 90%, 2.7 V ≤ VDD2 ≤ 3.6 V, C_{LOAD}= 15 pF		0.8	3	ns
		10% to 90%, 4.5 V ≤ VDD2 ≤ 5.5 V, C_{LOAD}= 15 pF		0.8	3	
t_f	DOUT fall time	90% to 10%, 2.7 V ≤ VDD2 ≤ 3.6 V, C_{LOAD}= 15 pF		0.8	3	ns
		90% to 10%, 4.5 V ≤ VDD2 ≤ 5.5 V, C_{LOAD}= 15 pF		0.8	3	
t_{ISTART}	Interface startup time	VDD2 at 3 V (min) to DOUT valid with VDD1 ≥ 3 V		32		CLKIN cycles
t_{ASTART}	Analog startup time	VDD1 step to 3.0 V with VDD2 ≥ 3 V, 0.1% settling		0.5		ms

(1) Provided by bench test or design simulation.

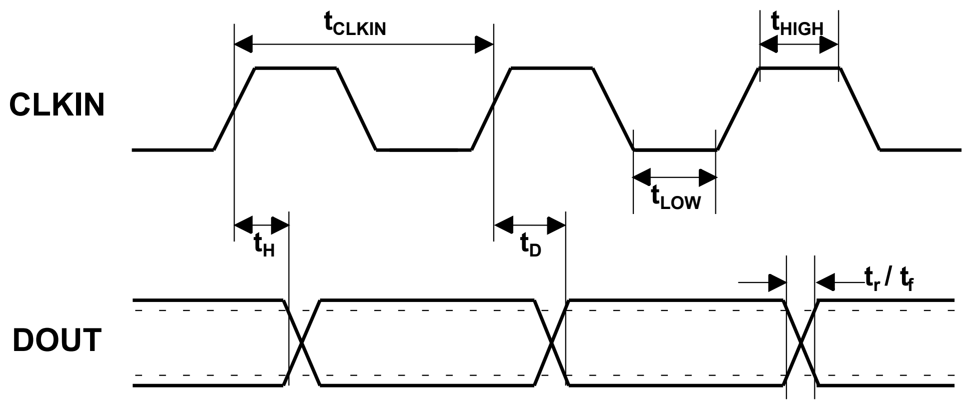


Figure 1. Digital Interface Timing of TPA8101 and TPA8102

Typical Performance Characteristics

All test conditions: VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV for TPA8101, VINP = –50 mV to 50 mV for TPA8102, VINN = 0 V, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256, unless otherwise noted.

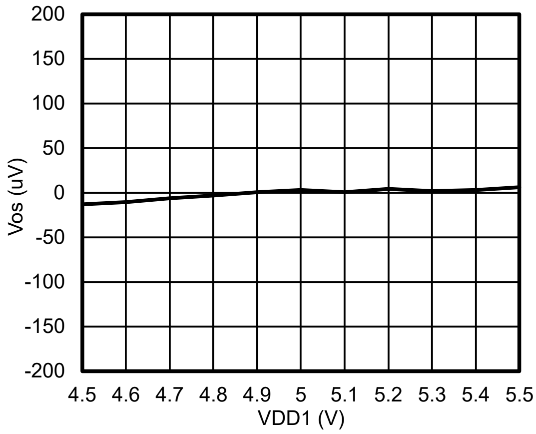


Figure 2. V_{OS} vs. VDD1

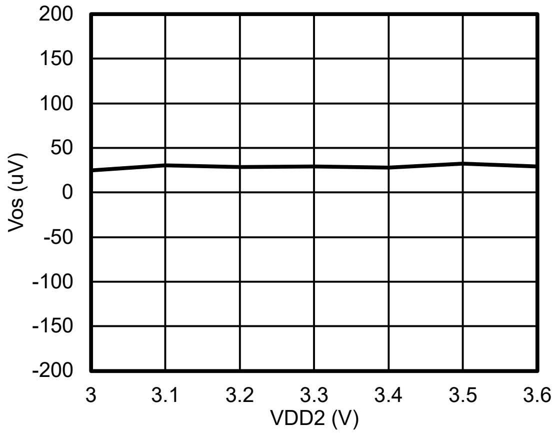


Figure 3. V_{OS} vs. VDD2

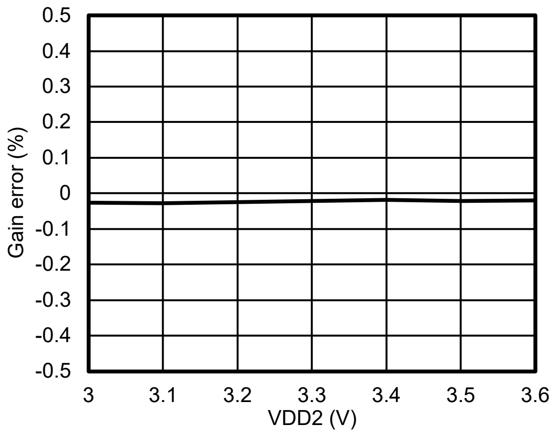


Figure 4. Gain Error vs. VDD2

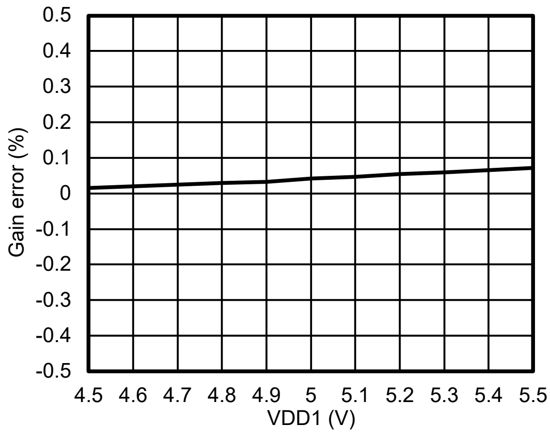


Figure 5. Gain Error vs. VDD1

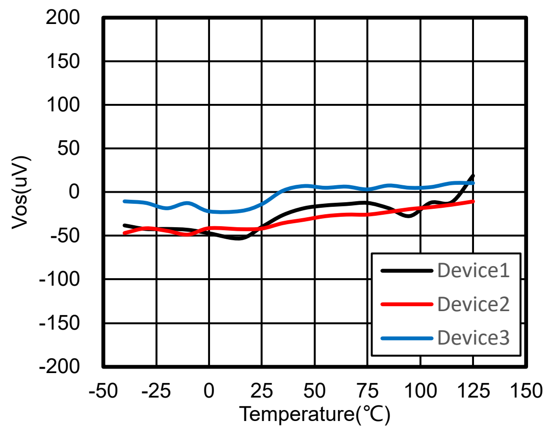


Figure 6. V_{OS} vs. Temperature of TPA8101

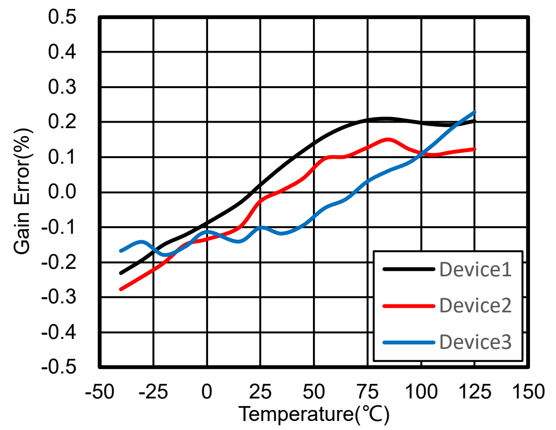


Figure 7. Gain Error vs. Temperature of TPA8101

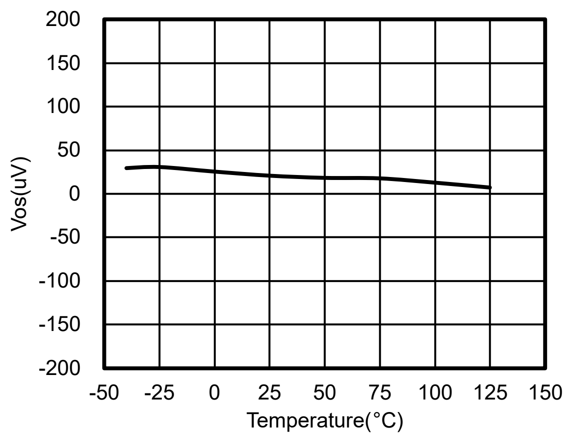


Figure 8. V_{OS} vs. Temperature of TPA8102

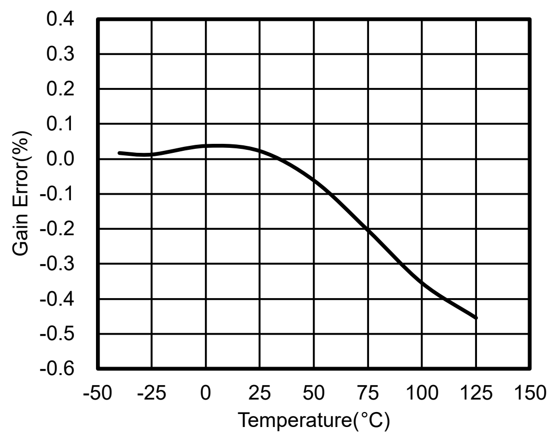


Figure 9. Gain Error vs. Temperature of TPA8102

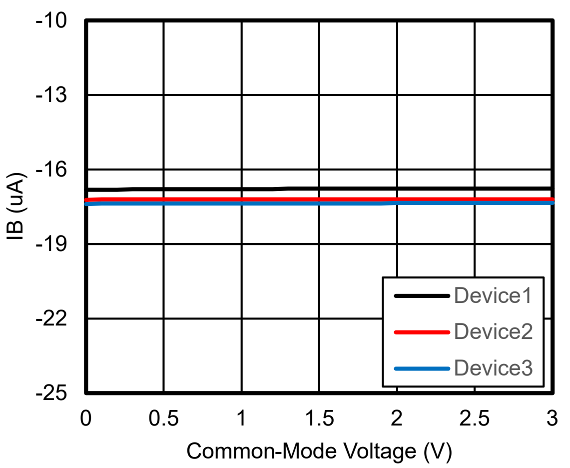


Figure 10. I_B vs. Common-Mode Voltage

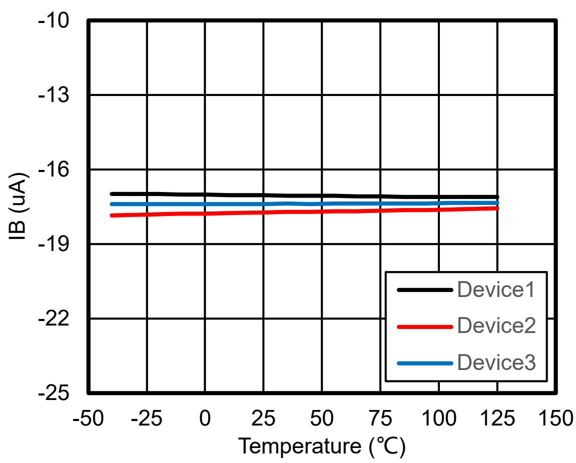


Figure 11. I_B vs. Temperature

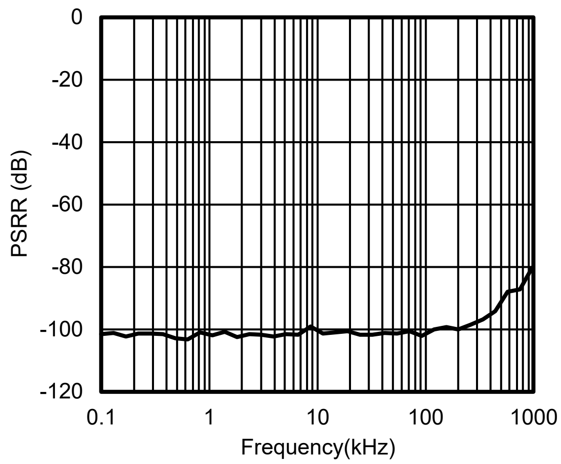


Figure 12. VDD1 PSRR vs. Frequency

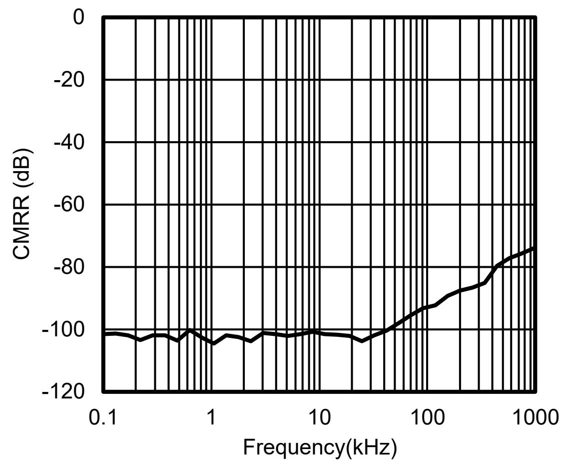


Figure 13. CMRR vs. Frequency

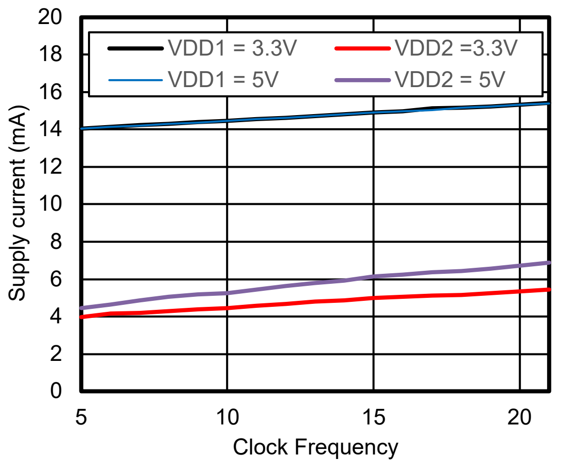


Figure 14. Supply Current vs. Clock Frequency

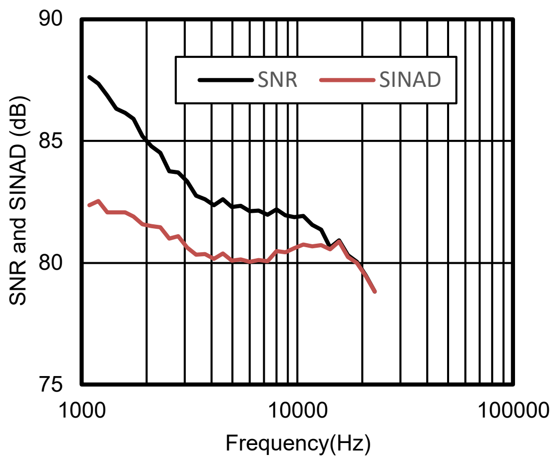


Figure 15. SNR and SINAD vs. Input Signal Frequency

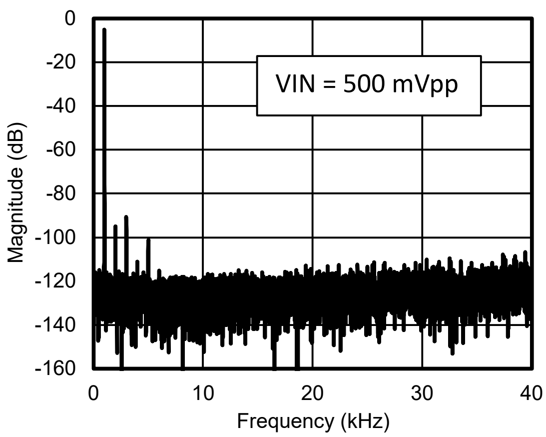


Figure 16. TPA8101 Frequency Spectrum with 1-kHz Input Signal

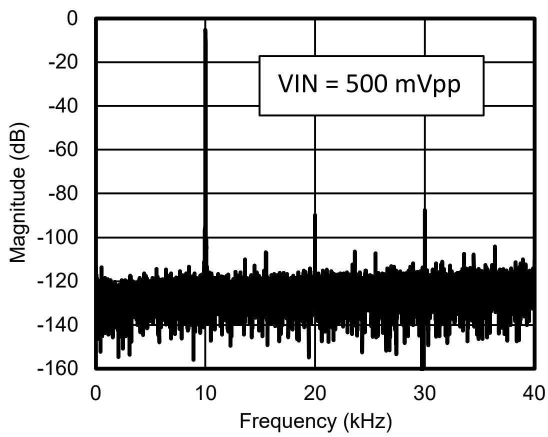


Figure 17. TPA8101 Frequency Spectrum with 10-kHz Input Signal

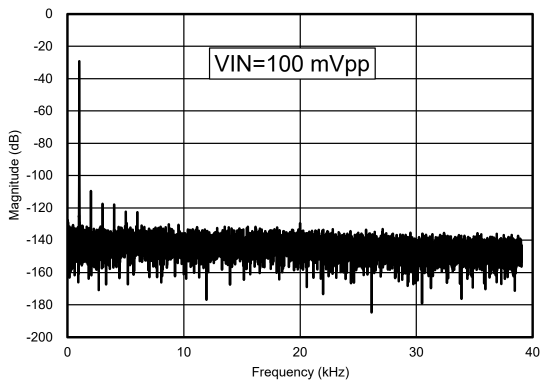


Figure 18. TPA8102 Frequency Spectrum with 1-kHz Input Signal

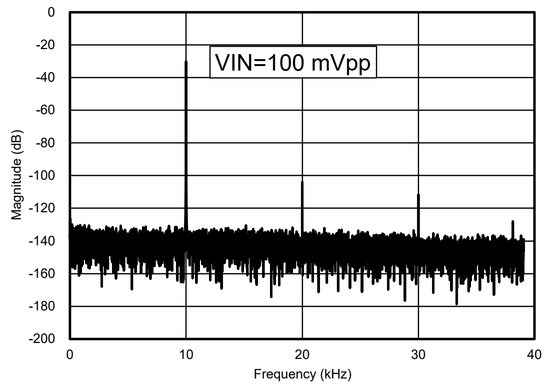


Figure 19. TPA8102 Frequency Spectrum with 10-kHz Input Signal

Detailed Description

Overview

The differential analog input of the device is a fully-differential amplifier feeding the switched-capacitor input of a delta-sigma (ΔΣ) modulator stage which digitizes the input signal into a 1-bit output stream. The isolated data output DOUT of the converter provides a stream of digital zeros and ones that are synchronous to the clock source at the CLKIN pin with a frequency in the range of 5 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

Based on the SiO_2-based and double-capacitive isolation barrier, the digital modulation and isolation barrier characteristics provide high reliability and common-mode transient immunity for the device.

Functional Block Diagram

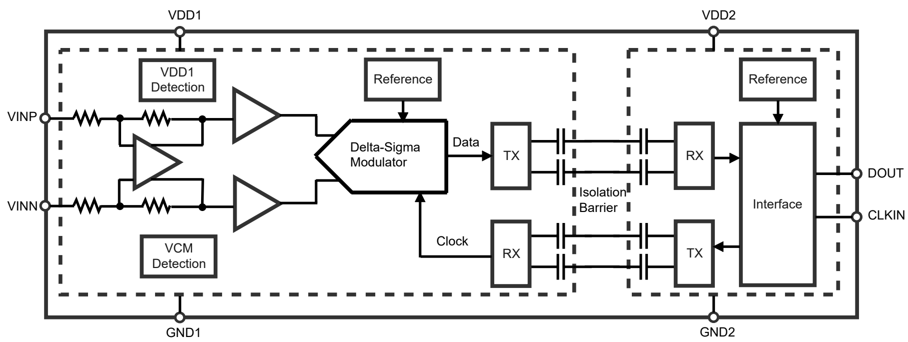


Figure 20. Functional Block Diagram

Feature Description

Fail-Safe Output

The device provides a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

• When the VDD1 is missing, or the voltage at VDD1 is lower than $VDD1_{UV}$ (the undervoltage detection threshold voltage of VDD1), the output DOUT of the device provides a steady-state bitstream of logic 0's.

• When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the V_{CMov} (the minimum common-mode overvoltage detection level), the output DOUT of the device provides a steady-state bitstream of logic 1's.

Output Behavior in Case of a Full-Scale Input

To distinguish from the output, if a full-scale input signal is applied to the device, the device generates a single one or zero every 128 bits at DOUT, depending on the polarity of the input signal.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

Figure 21 shows the typical application schematic.

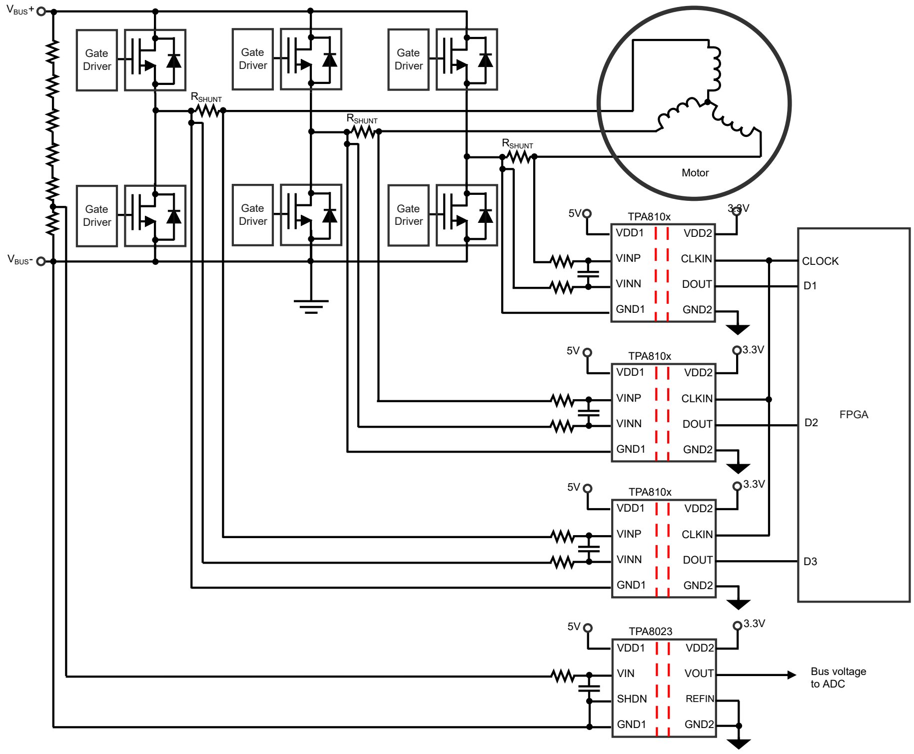


Figure 21. Application Schematic

Motor Drive Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, servo control systems, and other industrial applications.

The TPA810x is optimized for current sensing applications with shunt resistors. Figure 21 shows a typical operation of the device for current sensing in a motor drive application. Phase current is measured by the shunt resistors, R_{SHUNT}. The differential input and the high common-mode transient immunity of the device ensure reliable and accurate operation in high-noise environments.

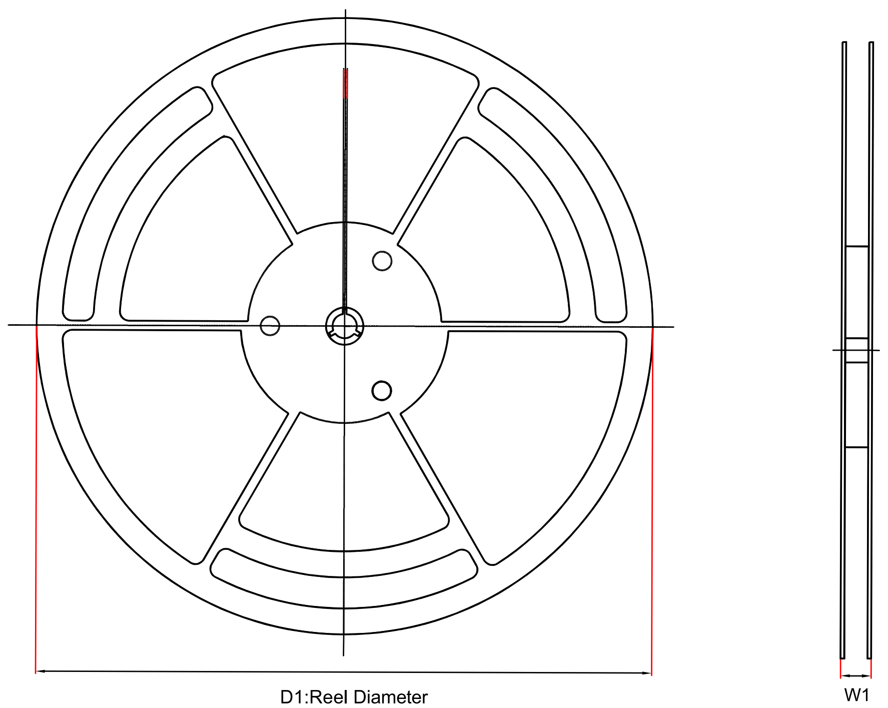
The DC bus voltage is measured by the TPA8023 with a high-impedance input and a wide input voltage range.

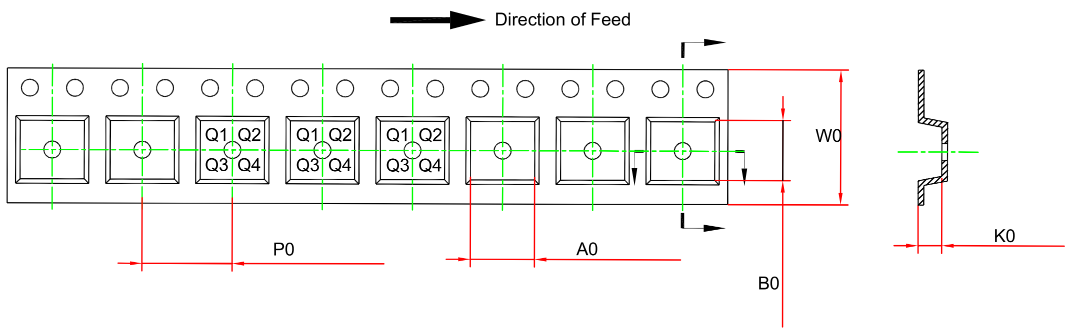
Power Supply Recommendation

In a typical frequency inverter application, the high-side power supply (VDD1) of the device is derived from the floating power supply of the upper gate driver. A Zener diode with a shunt resistor can be used to provide high-side power supply of the device, or a low-cost low-dropout regulator (LDO) may be used to reduce the noise on the power supply. Place a 0.1-μF bypass capacitor as close as possible to the VDD1 pin of the device for best performance, and an additional 1-μF to 10-μF capacitor may be used for better filtering.

To decouple the low-side power supply, place a 0.1-μF capacitor to the VDD2 pin of the device as close as possible, and an additional 1-μF to 10-μF capacitor may be used for better filtering.

Tape and Reel Information





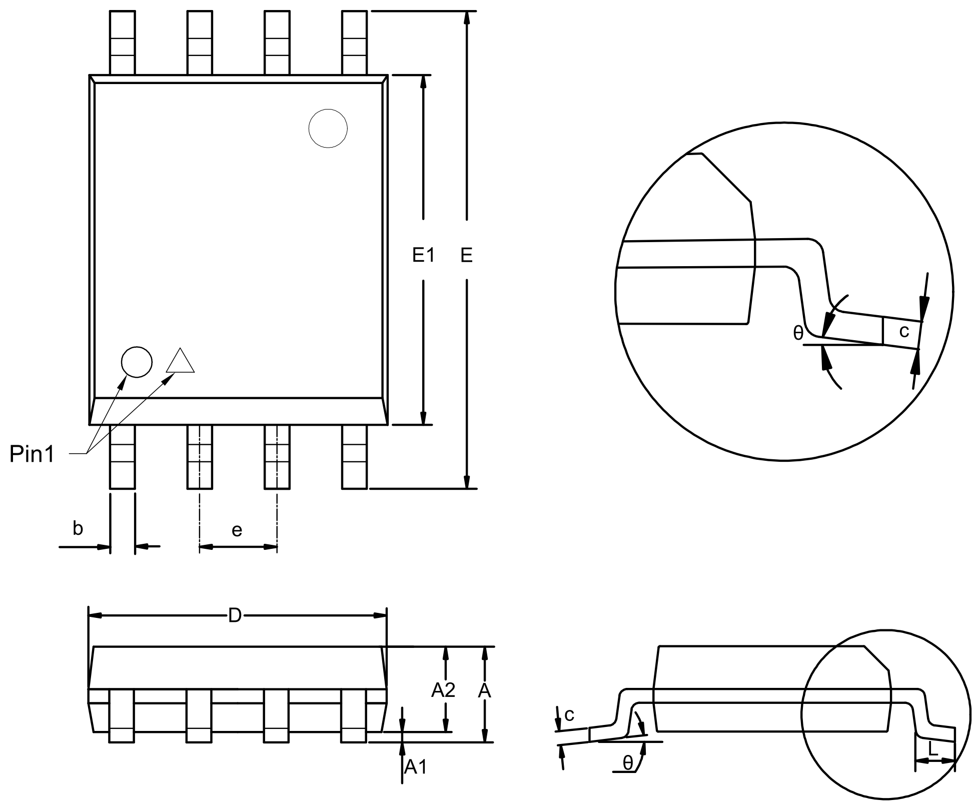
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA8101-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16.0	16.0	Q1
TPA8101-SOAR-S	WSOP8	330	21.6	11.95	6.2	3.1	16.0	16.0	Q1
TPA8101-TS1R	TSSOP8	330	17.6	6.7	3.4	1.7	8.0	12.0	Q1
TPA8101-SOBR	WSOP16	330	21.6	10.9	10.8	3.1	12.0	16.0	Q1
TPA8102-SOAR	WSOP8	330	21.6	11.95	6.2	3.1	16.0	16.0	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

WSOP8

Package Outline Dimensions SOA(WSOP-8-B)



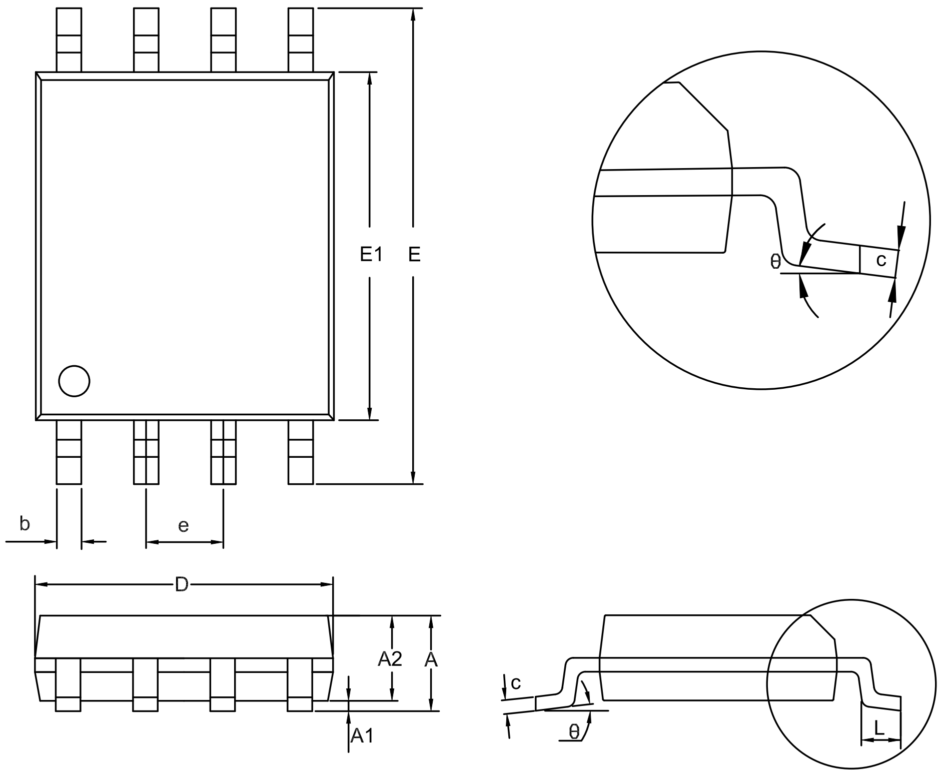
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.310	0.510	0.012	0.020
c	0.150	0.300	0.006	0.012
D	5.750	5.950	0.226	0.234
E	11.250	11.750	0.443	0.463
E1	7.400	7.600	0.291	0.299
e	1.270 BSC		0.050 BSC	
L	0.500	1.000	0.020	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP8

Package Outline Dimensions TS1(TSSOP-8-A)



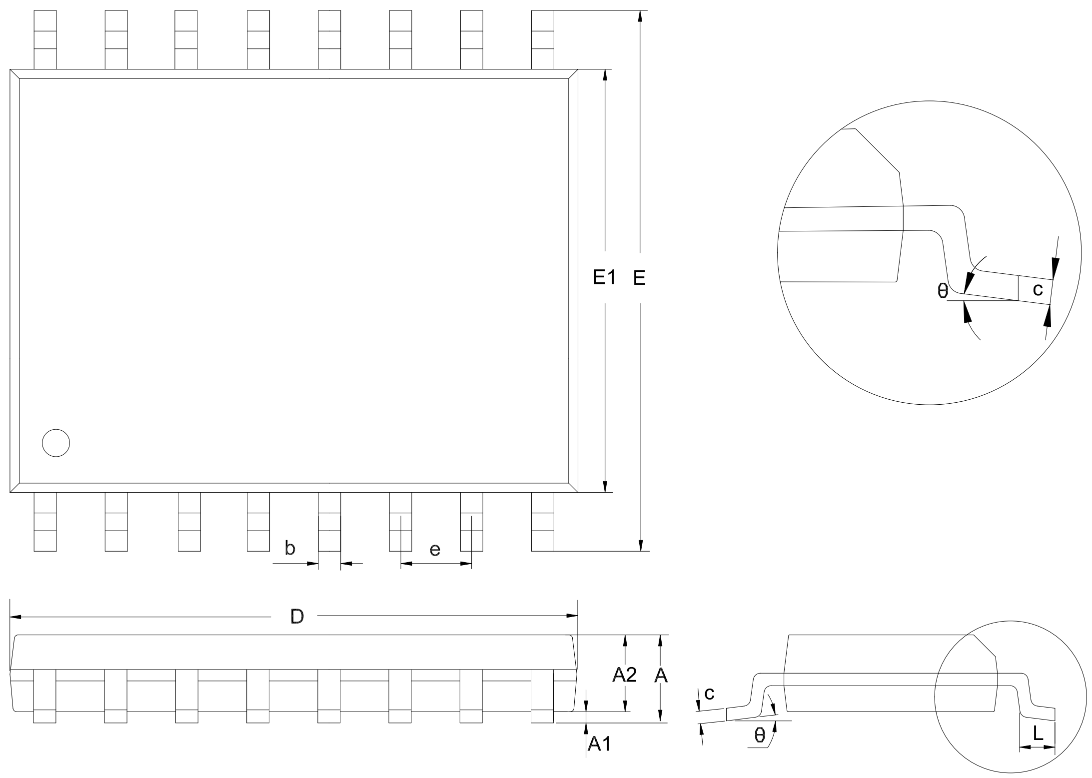
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

WSOP16

Package Outline Dimensions SOB(WSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
b	0.350	0.450	0.014	0.018
c	0.200	0.290	0.008	0.011
D	10.100	10.500	0.398	0.413
E	10.100	10.600	0.398	0.417
E1	7.300	7.700	0.287	0.303
e	1.270 BSC		0.050 BSC	
L	0.500	0.850	0.020	0.033
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA8101-SOAR	−40 to 125°C	WSOP8	A8101	3	Tape and Reel, 1000	Green
TPA8101-SOAR-S (1) (2)	−40 to 125°C	WSOP8	A8101	3	Tape and Reel, 1000	Green
TPA8101-TS1R	−40 to 125°C	TSSOP8	A8101	3	Tape and Reel, 3000	Green
TPA8101-SOBR	−40 to 125°C	WSOP16	A8101	3	Tape and Reel, 1500	Green
TPA8102-SOAR	−40 to 125°C	WSOP8	A8102	3	Tape and Reel, 1000	Green

(1) Passed AEC-Q100 Reliability Test.
(2) For future products, contact the 3PEAK factory for more information and samples.

Green: Defines "Green" to mean RoHS compatible and free of halogen substances.

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