140-dB Range (1 nA to 10 mA) Logarithmic Converter

Features

- 7 Full Decades of Range: 1 nA to 10 mA
- Functionally Support 100-pA Current Input
- Low Conformance Error: 0.2 dB from 10 nA to 10 mA
- Fast Step Response: Raising 0.2 μs, Falling 5 μs for 10-nA to 10-μA Input on INPT
- Basic Logarithmic Intercept at 100 pA
- Logarithmic Slope of 200 mV/20 dB (at the V_{LOG} Pin)
- Optimized for Fiber Optic Photodiode Interfacing
- Single-Supply Operation: 4.5 V to 5.5 V
- Power-down Mode

Applications

- High-Accuracy Optical Power Measurement
- Wide-Range Baseband Log Compression
- Versatile Detector for APC Loops
- EDFA

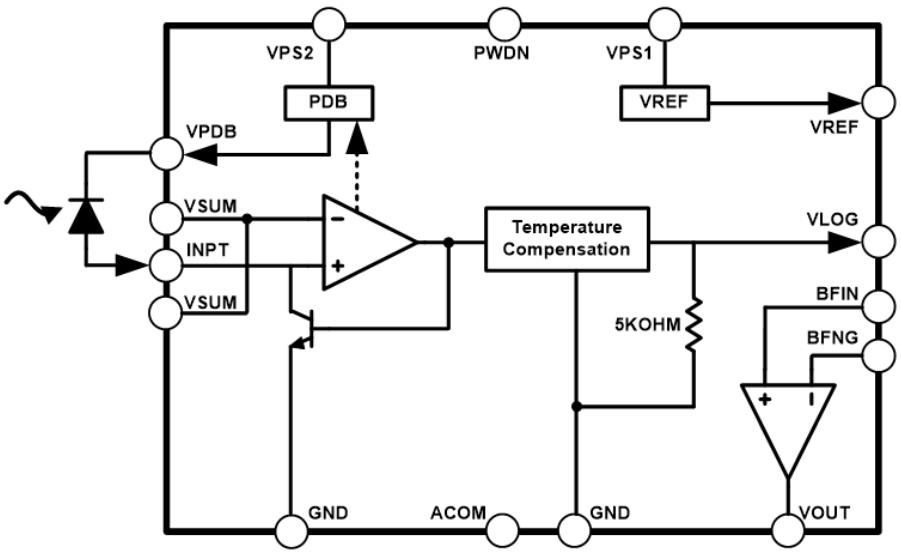
Description

The TPA8304 is a logarithmic detector optimized for the measurement of low-frequency signal power in fiber optic systems and offers a large dynamic range.

The wide measurement range, accuracy, and fast step response are achieved, which meets the requirements of an optic system.

The TPA8304 requires only a single positive supply of 5 V. The low quiescent current and chip disable facilitate are used in battery-operated applications.

Typical Application Circuit



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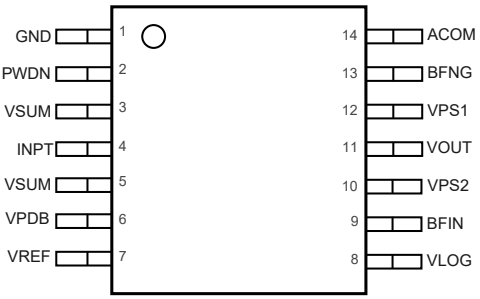
Revision History

Date	Revision	Notes
2019-09-10	Rev.Pre.0	Initial version.
2019-12-09	Rev.Pre.1	Added a new section in Application Information: Using the Fixed Bias.
2020-11-16	Rev.A.0	Added the Phase Margin and Gain Margin in Output Buffer, Pin BFIN, BFNG, V_{OUT} in Electrical Characteristics.
2021-05-30	Rev.A.1	Updated the Description.
2025-10-10	Rev.A.2	The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. • Updated to a new datasheet format. • Updated to a new format of Package Outline Dimensions. • Updated EC Tables : — Update the Min and Max value of Intercept. — Update the typical value of Minimum Output Voltage. — Update the typical value of Output Voltage Swing to Power and Ground. • Update Figures.

Pin Configuration and Functions

TPA8304
TSSOP14
Top View



TPA8304
QFN3x3-16
Top View

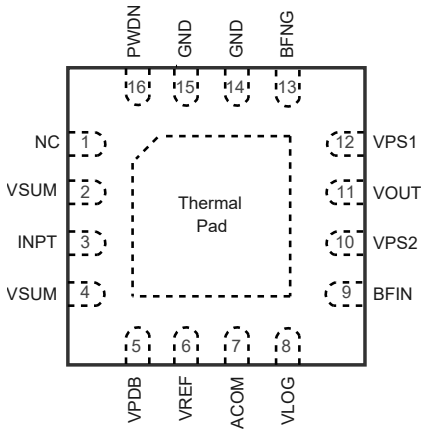


Table 1. Pin Functions: TPA8304

Pin No.		Name	I/O	Description
TSSOP14	QFN3x3-16			
1	14, 15	GND		Power supply ground connection.
2	16	PWDN	I	Power-down control input. The device is active when PWDN is taken low.
3, 5	2, 4	VSUM		Guard pins. They are used to shield the INPT current line.
4	3	INPT	I	Photodiode current input.
6	5	VPDB	O	Photodiode bias output. Connect this pin to the photodiode cathode when using adaptive bias control; Otherwise, leave this pin floating.
7	6	VREF	O	Voltage reference output of 2 V.
8	8	VLOG	O	Output of the logarithmic front-end processor.
9	9	BFIN	I	Buffer amplifier non-inverting input.
10	10	VPS2		Positive supply.
11	11	V_{OUT}	O	Buffer amplifier output.
12	12	VPS1		Positive supply.
13	13	BFNG	I	Buffer amplifier inverting input.
14	7	ACOM		Analog reference ground.
-	1	NC		The pins labeled NC can be allowed to float, but it is better to connect these pins to ground.
-	-	Thermal Pad		Thermal pad. Connect the thermal pad to the V_{SUM} pin to provide low leakage guard.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Supply Voltage		6.5	V
	Input Current to INPT (2)	−20	20	mA
T_J	Maximum Junction Temperature		125	°C
T_A	Operating Temperature Range	−40	85	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1), INPT Pin	500	V
		ANSI/ESDA/JEDEC JS-001 (1), All Other Pins except INPT	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV
LU	Latch Up	25 degrees	200	mA
		125 degrees	150	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3x3-16	75	54	°C/W
TSSOP14	180	35	°C/W

Electrical Characteristics

All test conditions: V_S = 5 V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
Power Supply, Pin V_{PS2}, V_{PS1}, GND							
V_S	Supply Voltage Range			4.5		5.5	V
I_Q	Quiescent Current per Amplifier				8	10	mA
I_{SN}	Shutdown Current	In disable state			40		μA
Input Interface, Pin INPT, V_{SUM}							
	Specified Current Range	Flows toward INPT		1			nA
					10	12	mA
	Functional Current Range (1)	Flows toward INPT			100		pA
	Input Node Voltage			1.05	1.2	1.35	V
	Input Node Voltage Drift				20		μV/°C
	V_{INPT} − V_{SUM}			−20		20	mV
Photodiode Bias, between Pin V_{PDB} and INPT							
	Minimum Value	IPD = 100 pA			100		mV
	Transresistance				150		mV/mA
Logarithmic Output, Pin V_{LOG}							
	Slope			195	200	205	mV/dec
			0°C to 70°C	192		208	mV/dec
	Intercept		0°C to 70°C	75	100	125	pA
			-40°C to 85°C	65		135	pA
	Low Conformance Error	10 nA < IPD < 10 mA, peak error			0.2	0.25	dB
		1 nA < IPD < 10 mA, peak error			0.5	0.75	dB
	Maximum Output Voltage	IPD = 10 mA			1.6		V
	Minimum Output Voltage	IPD ≤ 100 pA			0.002		V
	Output Resistance			4.95	5	5.05	kΩ
Reference Output, Pin V_{REF}							
	Output Voltage			1.96	2	2.04	V
			−40°C to 85°C	1.95		2.05	V
	Output Resistance				2		Ω
Output Buffer, Pin BFIN, BFNG, V_{OUT}							
V_{OS}	Input Offset Voltage			−10		10	mV

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
I_B	Input Bias Current				100		pA
	Output Voltage Swing to Power and Ground	No Load			3		mV
	Output Resistance				0.5		Ω
	Wideband Noise				1		μV/√Hz
	Small-Signal Bandwidth				10		MHz
SR	Slew Rate	0.2-V to 4.8-V output swing			15		V/μs
PM	Phase Margin	C_L = 100 pF			60		°
GM	Gain Margin	C_L = 100 pF			10		dB
Power-down Input, Pin PWDN							
	Logic Level, High State	V_S = 4.5 V to 5.5 V	−40°C to 85°C	2			V
	Logic Level, Low State	V_S = 4.5 V to 5. 5V	−40°C to 85°C			1	V

(1) Provided by the design simulation.

Step Response Time from Input to V_{LOG}, 0°C to 70°C							
	Rising Time			Falling Time			
Conditions	Min	Typ	Max	Min	Typ	Max	Unit
10 nA to 100 nA		2			4		μs
10 nA to 1 μA		0.5			3		μs
10 nA to 10 μA		0.2			5		μs
10 nA to 100 μA		0.2			10		μs
10 nA to 1 mA		0.2			15		μs

Typical Performance Characteristics

All test conditions: V_S = 5 V, unless otherwise noted.

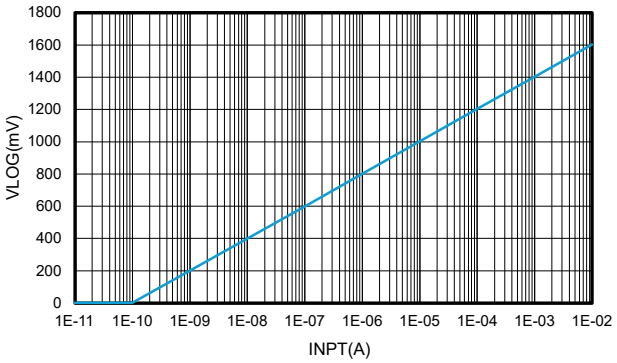


Figure 1. V_{LOG} Output Voltage vs. INPT Input Current

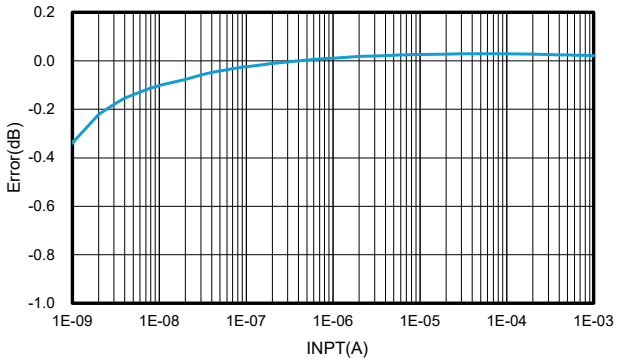


Figure 2. Law Conformance Error vs. INPT Input Current

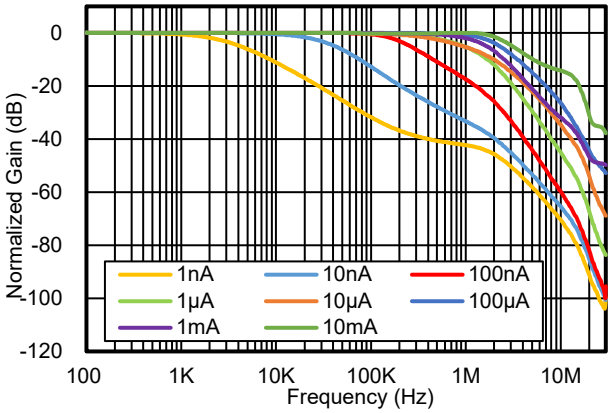


Figure 3. Normalized Small Signal Gain vs. Frequency

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Basic Configuration to Use the TPA8304

The basic configuration (see Figure 4) includes a 2.5x gain to amplify the V_{LOG} voltage by the buffer amplifier. This increases the slope of 10 mV/dB (200 mV/dec) at the V_{LOG} pin to 25 mV/dB (500 mV/dec) at V_{OUT}. For the full dynamic range of 140 dB, the output swing is 4.0 V, which can be accommodated by the rail-to-rail output stage when using the recommended 5-V supply.

The capacitor C1 and R1 at the INPT pin is not recommended to be assembled, because the TPA8304 uses advanced technology to ensure loop stability and fast step response. If C1 and R1 must be used to the ADI ADL5303 and AD8304 for compatibility, the recommended value is 470 pF for C1 and 750 Ω for R1, which can ensure larger output noise and slower step response than the unassembled configuration. The capacitor C_F from V_{LOG} to GND forms an optional single-pole low-pass filter. Since the resistance at this pin is 5 kΩ, a corner frequency of −3-dB can be realized to minimize output noise. A capacitor between V_{SUM} and GND is essential for minimizing the noise on this node. When the bias voltage at either V_{PDB} or V_{REF} is unnecessary, these pins should be left unconnected.

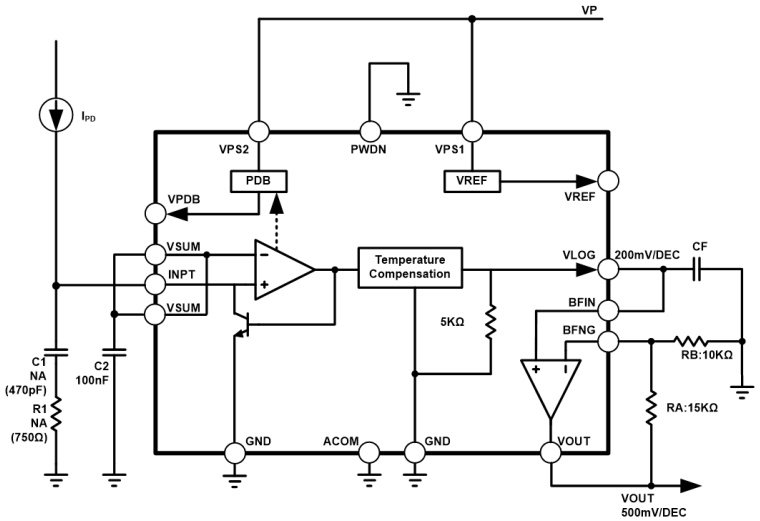


Figure 4. Basic Configuration

The relationship between the input current, IPD, applied to the INPT pin, and the voltage appearing at the V_{LOG} pin is:

$$V_{LOG} = V_Y \times LOG_{10}\left(\frac{I_{PD}}{I_Z}\right) \quad (1)$$

Where:

V_Y is the voltage slope (in the case of base-10 logarithms, it is also referred to as volts per decade).

I_Z is the fixed current in the logarithmic equation called the intercept.

In the basic configuration, the scaling is chosen so that V_Y is trimmed to 200 mV/decade (10 mV/dB). The intercept is positioned at 100 pA, and the output voltage, V_{LOG}, crosses zero when I_{PD} is of this value. However, the actual V_{LOG} must always be slightly above ground. Using Equation 1, the output for any value of I_{PD} can be calculated. For the specified input current of 1 nA to 10 mA of INPT:

$$1\ nA: V_{LOG} = 0.2\ V \log_{10}(1\ nA/100\ pA) = 0.2\ V$$

$$10\ mA: V_{LOG} = 0.2\ V \log_{10}(10\ mA/100\ pA) = 1.6\ V$$

In practice, both the slope and intercept can be altered, to either higher or lower values, without any significant loss of calibration accuracy, by using one or two external resistors, often in conjunction with the 2-V voltage reference at the V_{REF} pin.

Using the Adaptive Bias

For most photodiode applications, the placement of the anode above ground is acceptable in some cases, as long as the positive bias on the cathode is enough to support the peak current for a particular diode, limited by its series resistance. To address this matter, the TPA8304 provides a diode bias that increases linearly with the input current. This bias voltage appears at the V_{PDB} pin, and varies from 1.3 V (reverse-biasing the diode by 0.1 V) for I_{PD} = 100 pA and rises to 2.8 V (for a diode bias of 1.7 V) at I_{PD} = 10 mA. The adaptive biasing function is valuable in minimizing the dark current while preventing the loss of photodiode bias at high currents. The use of the adaptive bias feature is shown in Figure 5.

The capacitor C_{PB}, between the photodiode cathode at the V_{PDB} pin and GND, is used to lower the impedance at this node and improve the high-frequency accuracy at current levels where the bandwidth of the TPA8304 is high. C_{PB} also provides a high-frequency path for any high-frequency modulation on the optical signal. A suitable C_{BP} value (1 nF to 33 nF) is recommended in practice for the fast-falling step response. An undershoot appears at the output in the V_{LOG} pin when inputting a large-falling step (for example, 1 mA to 1 nA) if a large CPB value (> 33 nF) is used.

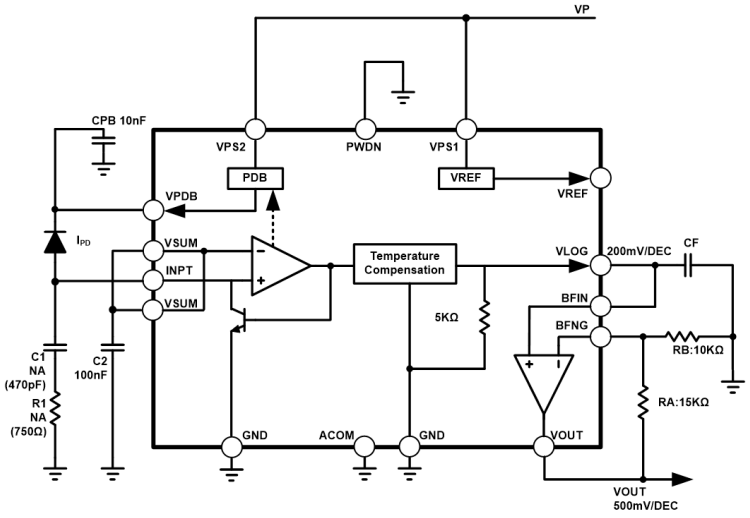


Figure 5. Using the Adaptive Bias

Using the Fixed Bias

For some photodiode applications, the fixed bias voltage is used for a photodiode. As the INPT pin has an around 1.2-V voltage, the voltage cross the photodiode must be carefully considered, especially during power-off or power-on of the chip. The current of the photodiode must be limited to the value of the rating current, otherwise, the photodiode may be damaged by the large current, (see Figure 6). To keep the photodiode safe, the system design should be guaranteed:

- Always keep the voltage of V_{BIAS} equal to or larger than V_P (the power supply of the TPA8304), especially during power-off or power-on. The same source for V_{BIAS} and V_P is recommended.
- Or, use the resistor R_{LIMIT} to limit the current of the photodiode to a afe value if the previous solution is unavailable.

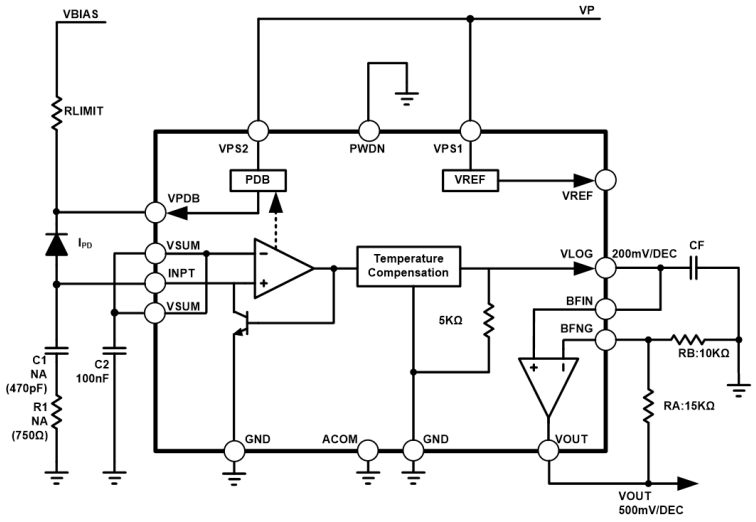


Figure 6. Using the Fixed Bias

Typical Application

Figure 7 shows the typical application schematic.

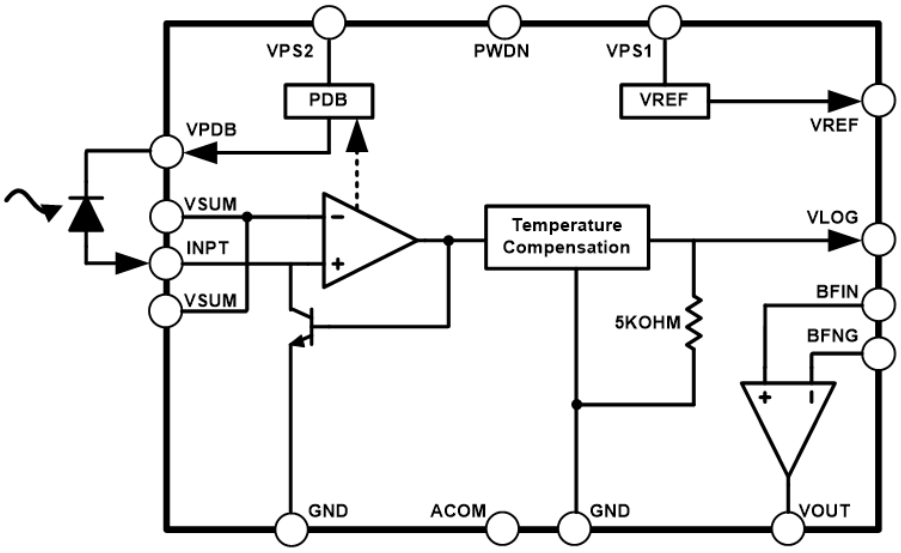
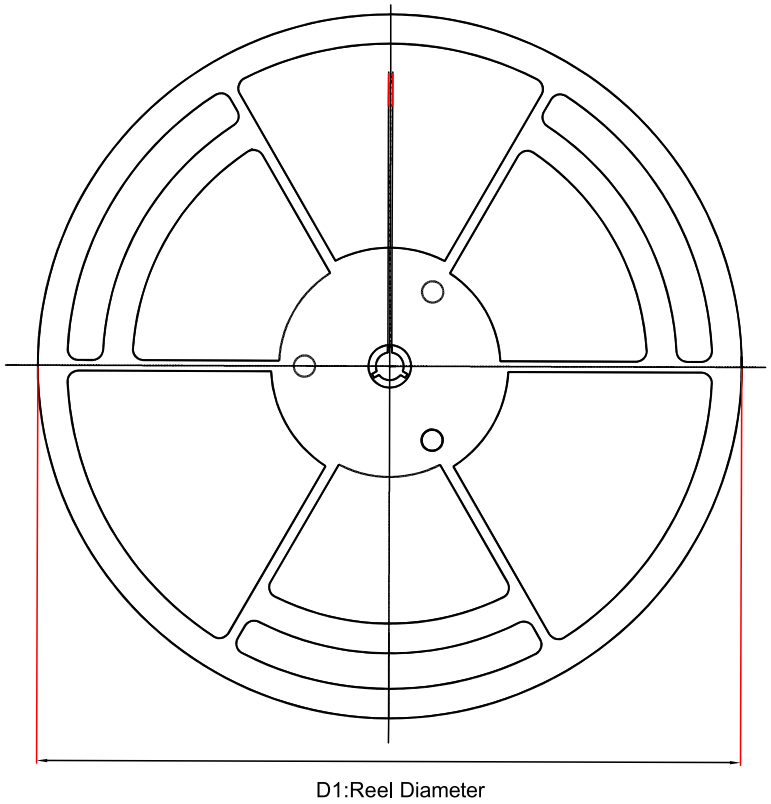
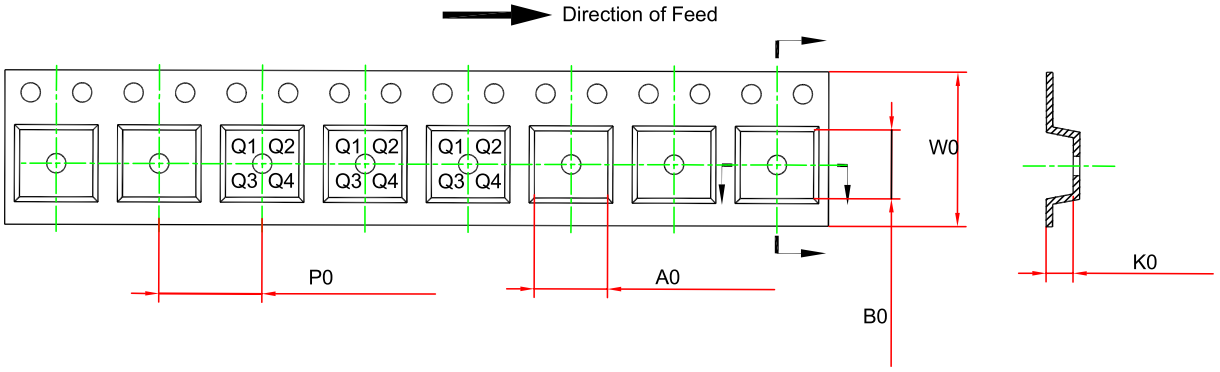


Figure 7. Typical Application Circuit

Tape and Reel Information



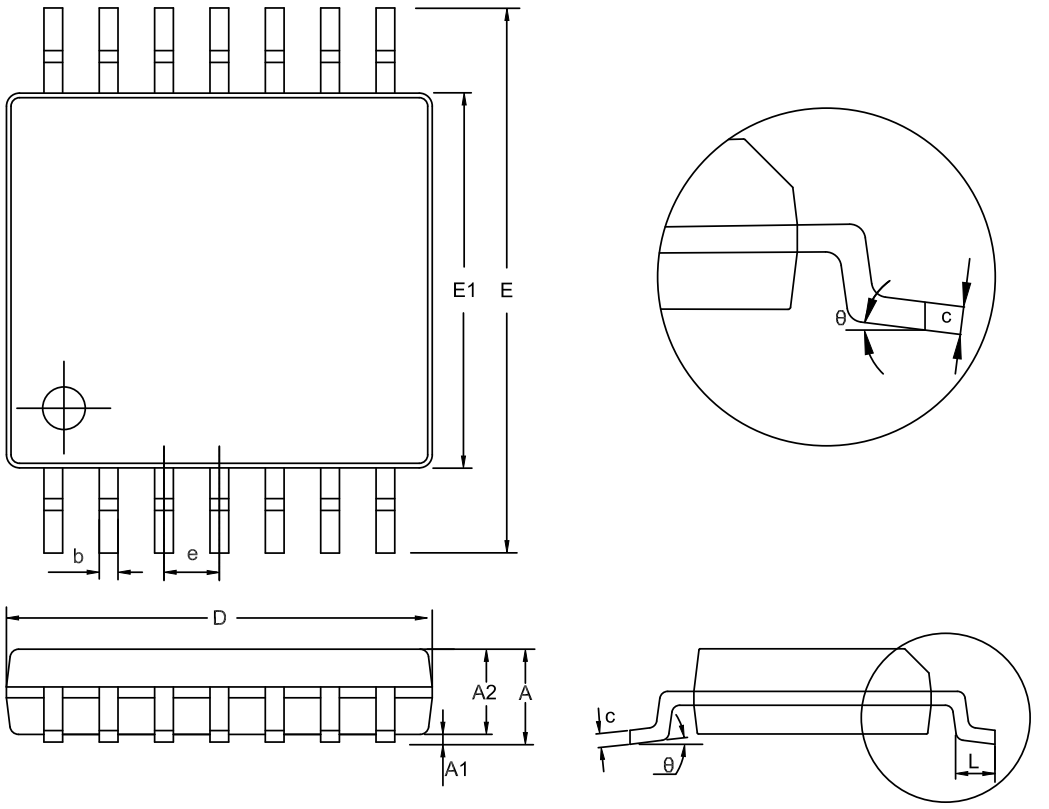


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA8304-TS2R-S	TSSOP14	330	17.6	6.8	5.5	1.5	8	12	Q1
TPA8304-QF4R	QFN3X3-16	330	16.6	3.2	3.2	1.1	8	12	Q1
TPA8304-QF4R-S	QFN3X3-16	330	16.6	3.2	3.2	1.1	8	12	Q1

Package Outline Dimensions

TSSOP14

Package Outline Dimensions TS2(TSSOP-14-A)



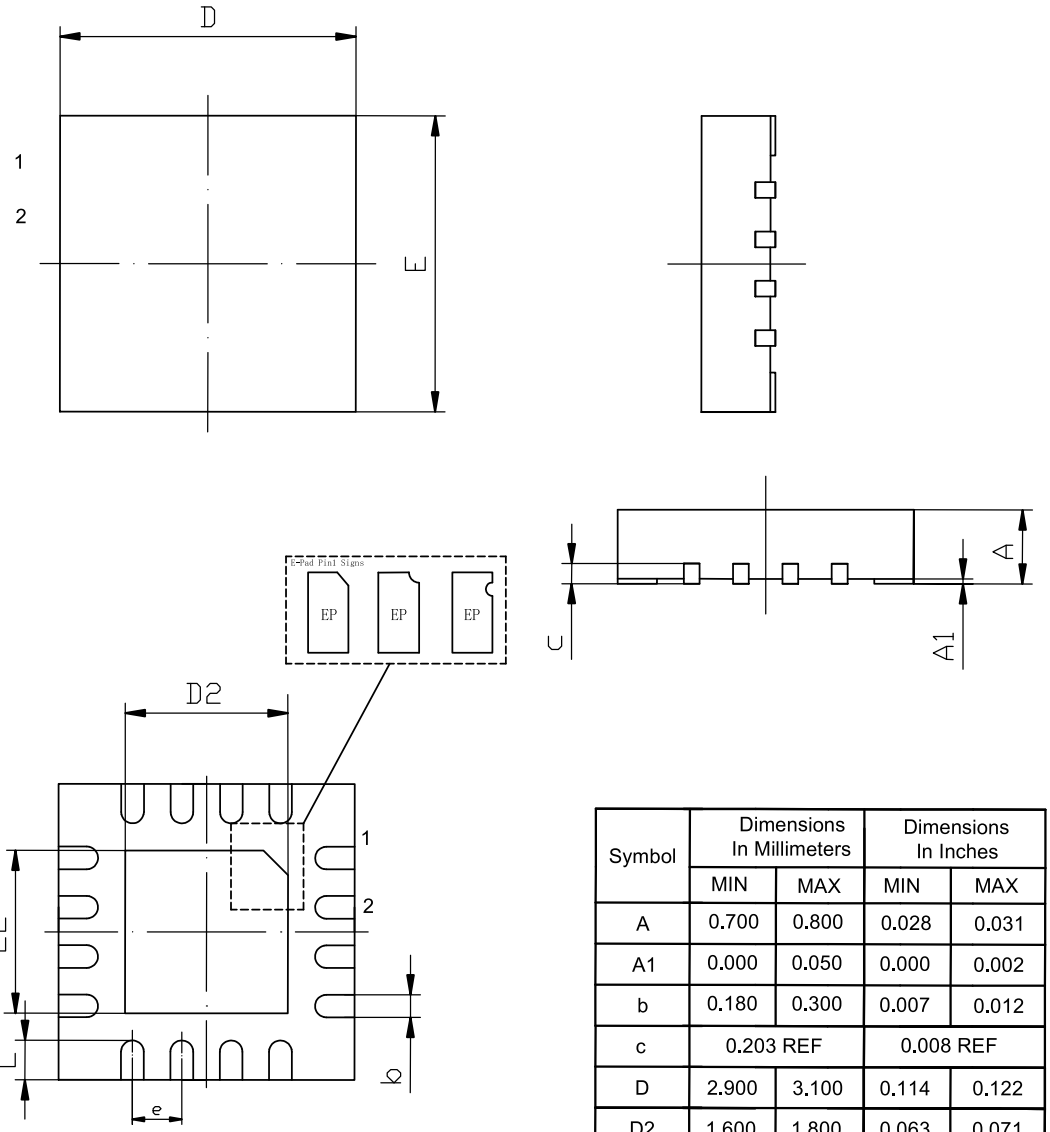
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

QFN3X3-16

Package Outline Dimensions QFN(QFN3X3-16-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D2	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E2	1.600	1.800	0.063	0.071
e	0.500 BSC		0.020 BSC	
L	0.250	0.500	0.010	0.020

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA8304-TS2R-S	−40 to 85°C	TSSOP14	A8304	3	Tape and Reel, 3000	Green
TPA8304-QF4R	−40 to 85°C	QFN3×3-16	A8304	3	Tape and Reel, 4000	Green
TPA8304-QF4R-S	−40 to 85°C	QFN3×3-16	A8304	3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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