

2-mm x 2-mm 小外形尺寸无引线 (SON) 封装内的 3-MHz 2-A 降压转换器

 查询样品: [TLV62065-Q1](#)

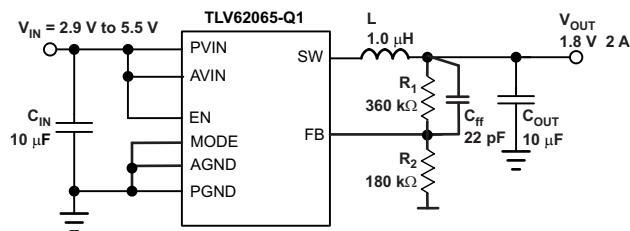
特性

- 符合汽车应用要求
- 具有下列结果的 **AEC-Q100** 测试指南:
 - 器件温度 2 级: **-40°C 至 105°C** 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 **H2**
 - 器件充电器件模型 (CDM) ESD 分类等级 **C3B**
- V_{IN} 范围从 **2.9 V 至 5.5 V**
- 效率高达 **97%**
- 省电模式 / MHz 固定脉宽调制 (PWM) 模式
- PWM 模式中的输出电压准确度为 **±2.0%**
- 输出放电功能
- 典型值为 **18µA** 的静态电流
- 针对最低压降的 **100%** 占空比
- 要获得改进的特性集, 请见 **TPS62065**
- 采用 **2-mm x 2-mm x 0.75-mm SON** 封装

应用范围

- 负载点 (POL)
- 笔记本电脑、掌上电脑
- 便携式媒体播放器
- 机顶盒

TYPICAL APPLICATION CIRCUIT



说明

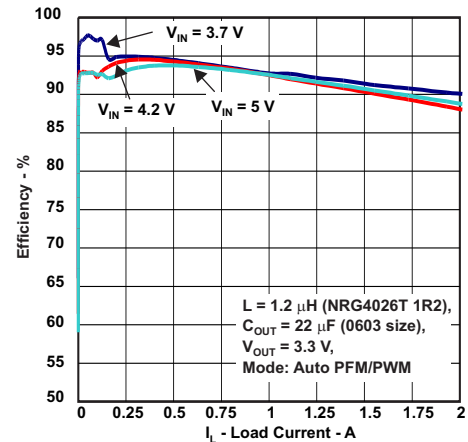
TLV62065-Q1 是一款具有 1.2-V 固定输出电压的高效、同步降压、dc-dc 转换器。它提供高达 2 A 的输出电流。

借助于 2.9 V 至 5.5 V 的输入电压范围, 此器件非常适合用于针对 5-V 或者 3.3-V 系统电源轨的电源转换。TLV62065-Q1 运行在 3-MHz 固定频率下并在轻负载电流时进入省电模式运行以保持整个负载电流范围内的高效率。对于低噪声应用, 通过将 MODE 引脚上拉至高电平, 可强制 TLV62065-Q1 进入固定频率 PWM 模式。

在关断模式下, 流耗减至少于 1µA 并且一个内部电路将输出电容器放电。

TLV62065-Q1 具有 1-µH 电感器和 10-µF 输出电容器。

TLV62065-Q1 采用 2-mm x 2-mm x 0.75-mm 8-引脚 SON 封装。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012, Texas Instruments Incorporated
 English Data Sheet: [SLVSB92](#)

TLV62065-Q1

ZHCS783A – JANUARY 2012 – REVISED MARCH 2012

www.ti.com.cn


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	WSON -DSG	Reel of 3000	TLV62065TDSGRQ1	SCD

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE		UNIT
		MIN	MAX	
Voltage range ⁽²⁾	AVIN, PVIN	–0.3	7	V
	EN, MODE, FB	–0.3 to	V _{IN} + 0.3 < 7	
	SW	–0.3	7	
Current (source)	Peak output	Internally limited		A
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B		750	V
Temperature	T _J	–40	140	°C
	T _{stg}	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.

THERMAL INFORMATION

THERMAL METRIC		TLV62065-Q1		UNITS
		DSG		
		8 PINS		
θ _{JA}	Junction-to-ambient thermal resistance	92.2		°C/W
θ _{JC(top)}	Junction-to-case(top) thermal resistance	70.4		
θ _{JB}	Junction-to-board thermal resistance	46.6		
ψ _{JT}	Junction-to-top characterization parameter	1.7		
ψ _{JB}	Junction-to-board characterization parameter	46.3		
θ _{JC(bottom)}	Junction-to-case(bottom) thermal resistance	39.7		

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN} , PV_{IN}	Supply voltage	2.9		5.5	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		V_{IN}	V
L	Effective inductance range	0.7	1	1.6	μ H
C_{OUT}	Effective output-capacitance range	4.5	10	22	μ F
T_A	Operating ambient temperature ⁽¹⁾	-40		105	°C
T_J	Operating junction temperature	-40		140	°C

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

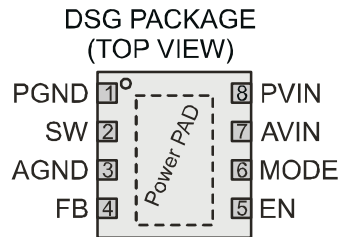
ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at $T_A = 25^\circ\text{C}$. Unless otherwise noted, specifications apply for condition $V_{IN} = EN = 3.6\text{ V}$. External components $C_{IN} = 10\ \mu\text{F}$ 0603, $C_{OUT} = 10\ \mu\text{F}$ 0603, $L = 1\ \mu\text{H}$, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		5.5	V
I_Q	Operating quiescent current	$I_{OUT} = 0\text{ mA}$, device operating in PFM mode and not device not switching		18		μA
I_{SD}	Shutdown current	$EN = \text{GND}$, current into AVIN and PVIN combined		0.1	5	μA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High-level input voltage	$2.9\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	1		5.5	V
V_{IL}	Low-level input voltage	$2.9\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	0		0.4	V
I_{IN}	Input bias current	EN, MODE tied to GND or AVIN		0.01	1	μA
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on-resistance	$V_{IN} = 3.6\text{ V}^{(1)}$		120	180	$\text{m}\Omega$
		$V_{IN} = 5\text{ V}^{(1)}$		95	150	
$r_{DS(on)}$	Low-side MOSFET on-resistance	$V_{IN} = 3.6\text{ V}^{(1)}$		90	130	$\text{m}\Omega$
		$V_{IN} = 5\text{ V}^{(1)}$		75	100	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	$3\text{ V} \leq V_{IN} \leq 3.6\text{ V}$	2300	2750		mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		$^\circ\text{C}$
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OSCILLATOR						
f_{SW}	Oscillator frequency	$2.9\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	2.6	3	3.4	MHz
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage, PWM mode	PWM operation, $\text{MODE} = V_{IN}$, $2.9\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, 0-mA load	-2.0	0	2.0	%
$V_{FB(PFM)}$	Feedback voltage, PFM mode, voltage positioning	Device in PFM mode, voltage positioning active ⁽²⁾		1		
V_{FB}	Load regulation			-0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with $EN = \text{GND}$, $2.9\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $0.8\text{ V} \leq V_{OUT} \leq 3.6\text{ V}$		200		Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		μs

(1) Maximum value applies for $T_J = 85^\circ\text{C}$.

(2) In PFM mode, the internal reference voltage is set to typ. $1.01 \times V_{ref}$. See the parameter measurement information.

PIN ASSIGNMENTS

TERMINAL FUNCTIONS

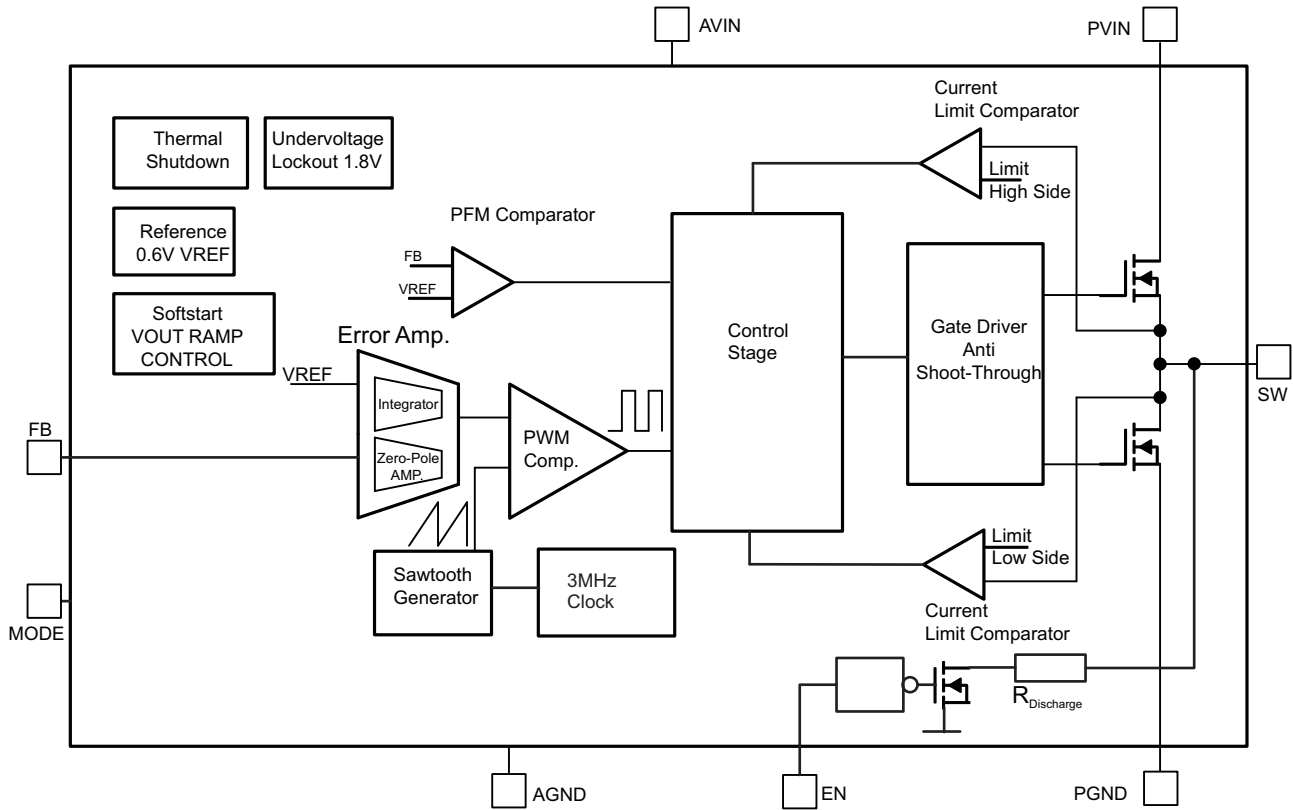
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	3	IN	Analog GND supply pin for the control circuit.
AV _{IN}	7	IN	Analog V _{IN} power supply for the control circuit. Must be connected to PVIN and input capacitor.
EN	5	IN	This is the enable pin of the device. Pulling this pin low forces the device into shutdown mode. Pulling this pin high enables the device. This pin must be terminated.
FB	4	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In the case of fixed output voltage option, connect this pin directly to the output capacitor.
MODE	6	IN	MODE pin = high forces the device to operate in fixed-frequency PWM mode. MODE pin = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode. This pin must be terminated.
PGND	1	PWR	GND supply pin for the output stage
PV _{IN}	8	PWR	V _{IN} power-supply pin for the output stage
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
Thermal pad	–	–	For good thermal performance, this pad must be soldered to the land pattern on the PCB. This pad should be used as device GND.

TLV62065-Q1

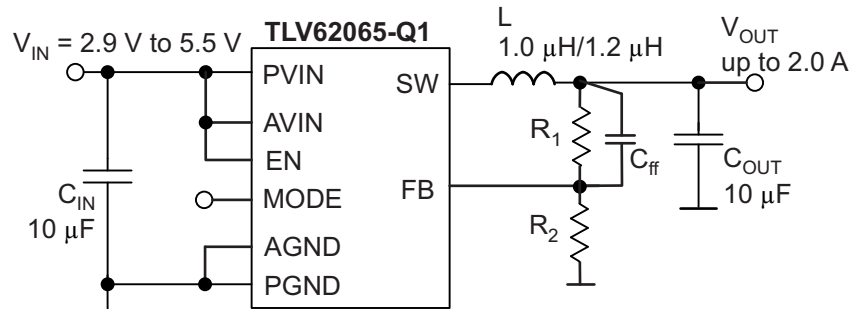
ZHCS783A – JANUARY 2012 – REVISED MARCH 2012

www.ti.com.cn

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L: LQH44PN1R0NP0, L = 1.0 μ H, Murata,
 NRG4026T1R2, L = 1.2 μ H, Taiyo Yuden
 C_{IN}/C_{OUT} : GRM188R60J106U, Murata 0603 size

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

		FIGURE
η Efficiency	Load Current, $V_{OUT} = 1.2$ V, Auto PF//PWM Mode, Linear Scale	Figure 1
	Load Current, $V_{OUT} = 1.8$ V, Auto PFM/PWM Mode, Linear Scale	Figure 2
	Load Current, $V_{OUT} = 3.3$ V, PFM/PWM Mode, Linear Scale	Figure 3
	Load Current, $V_{OUT} = 1.8$ V, Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale	Figure 4
Output Voltage Accuracy	Load Current, $V_{OUT} = 1.8$ V, Auto PFM/PWM Mode	Figure 5
	Load Current, $V_{OUT} = 1.8$ V, Forced PWM Mode	Figure 6
Shutdown Current	Input Voltage and Ambient Temperature	Figure 7
Quiescent Current	Input Voltage	Figure 8
Oscillator Frequency	Input Voltage	Figure 9
Static Drain-Source On-State Resistance	Input Voltage, Low-Side Switch	Figure 10
	Input Voltage, High-Side Switch	Figure 11
$R_{DISCHARGE}$	Input Voltage vs. V_{OUT}	Figure 12
Typical Operation	PWM Mode, $V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V, 500 mA, $L = 1.2$ μ H, $C_{OUT} = 10$ μ F	Figure 13
	PFM Mode, $V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V, 20 mA, $L = 1.2$ μ H, $C_{OUT} = 10$ μ F	Figure 14
Load Transient	PWM Mode, $V_{IN} = 3.6$ V, $V_{OUT} = 1.2$ V, 0.2 mA to 1 A	Figure 15
	PFM Mode, $V_{IN} = 3.6$ V, $V_{OUT} = 1.2$ V, 20 mA to 250 mA	Figure 16
	$V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V, 200 mA to 1500 mA	Figure 17
Line Transient	PWM Mode, $V_{IN} = 3.6$ V to 4.2 V, $V_{OUT} = 1.8$ V, 500 mA	Figure 18
	PFM Mode, $V_{IN} = 3.6$ V to 4.2 V, $V_{OUT} = 1.8$ V, 500 mA	Figure 19
Startup into Load	$V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V, Load = 2.2- Ω	Figure 20
Output Discharge	$V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V, No Load	Figure 21

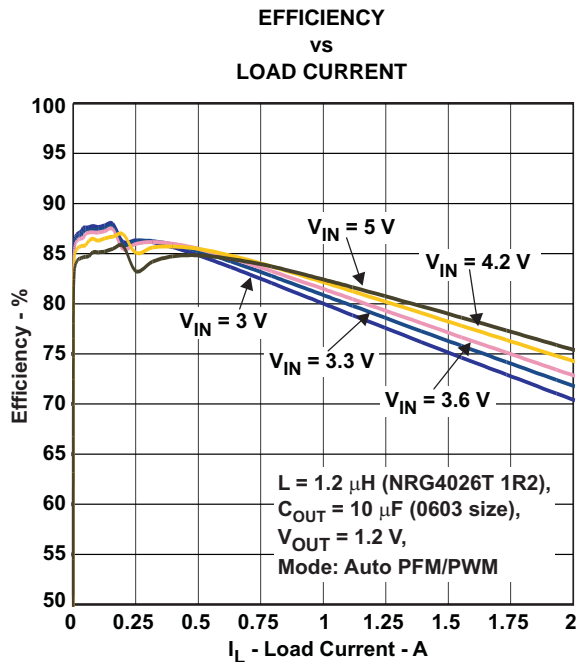


Figure 1. $V_{OUT} = 1.2$ V, Auto PFM/PWM Mode, Linear Scale

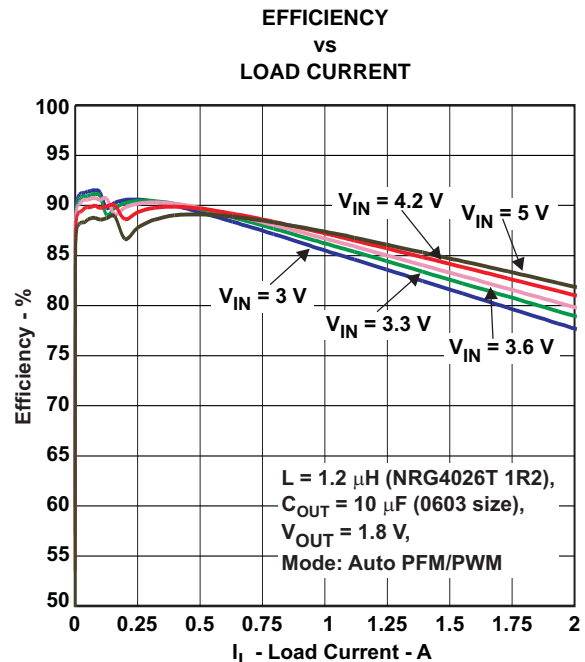


Figure 2. $V_{OUT} = 1.8$ V, Auto PFM/PWM Mode, Linear Scale

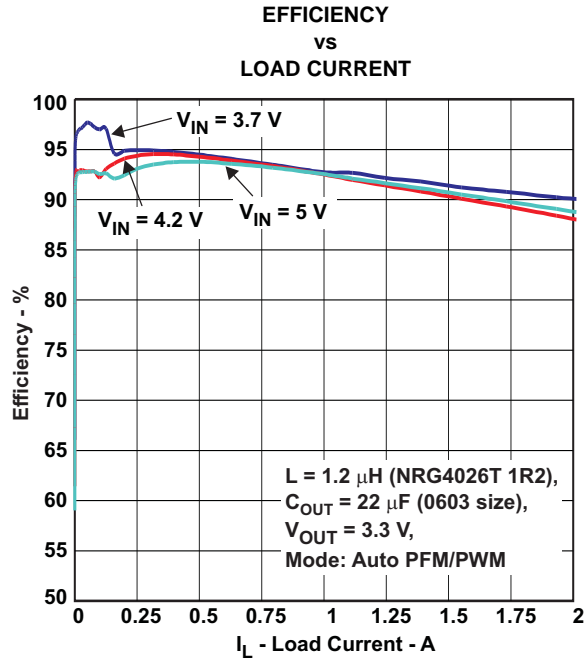


Figure 3. $V_{OUT} = 3.3V$, Auto PFM/PWM Mode, Linear Scale

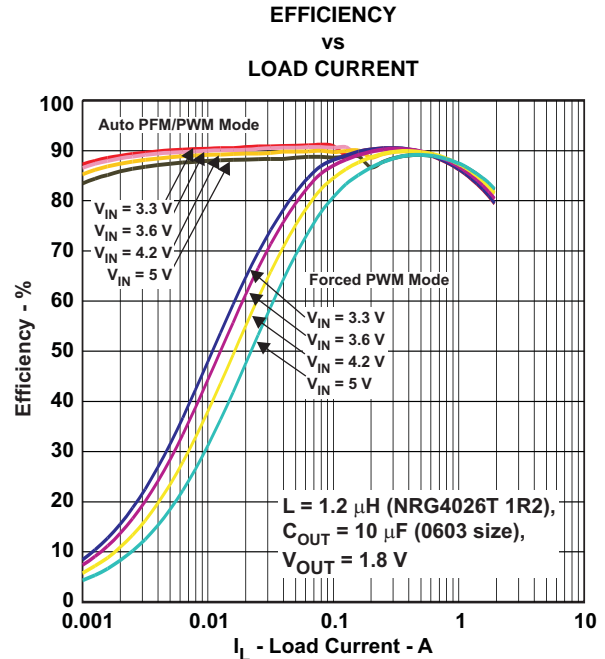


Figure 4. Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale

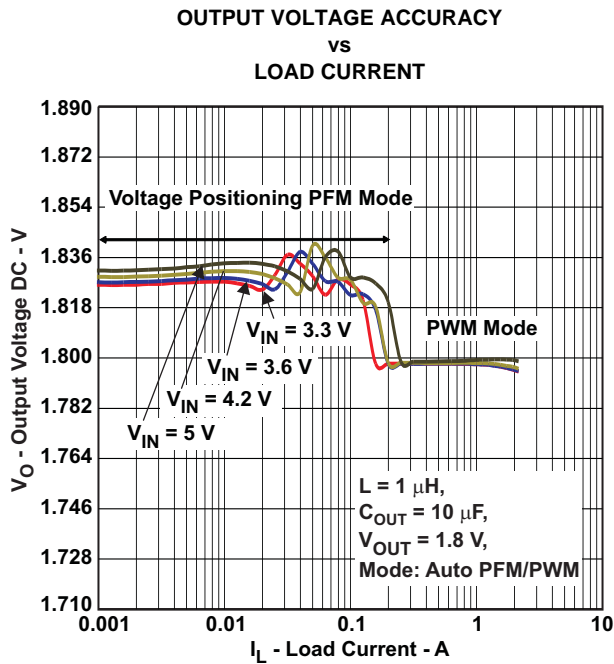


Figure 5. Auto PFM/PWM Mode

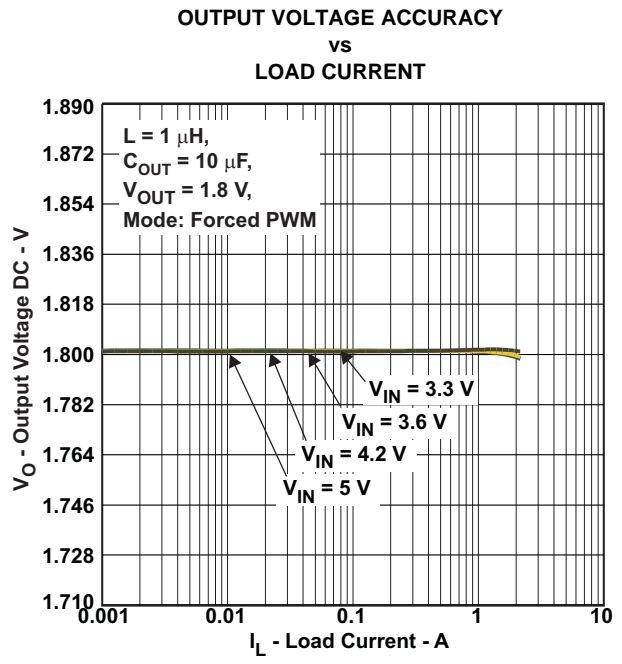


Figure 6. Forced PWM Mode

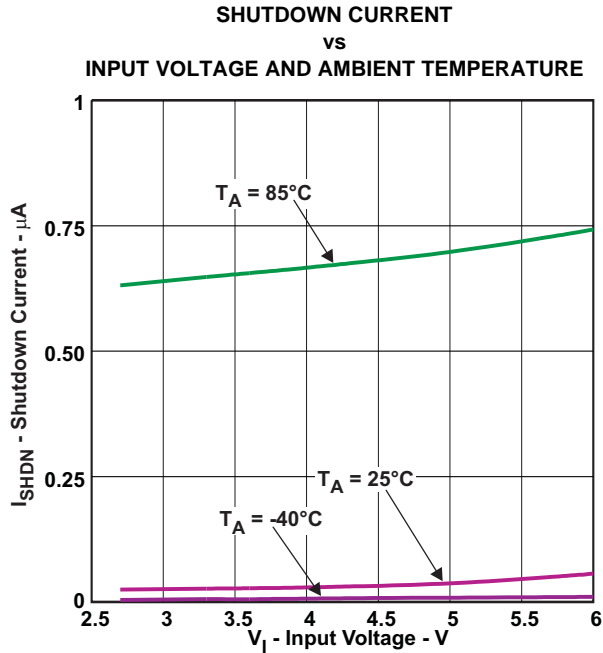


Figure 7.

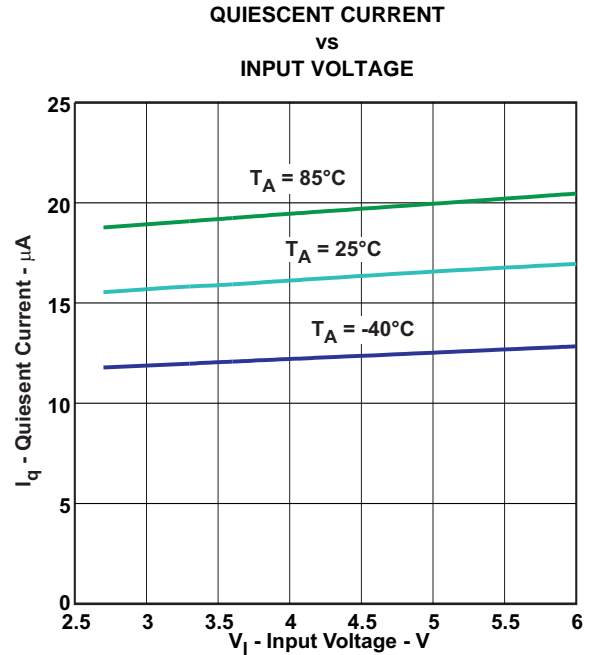


Figure 8.

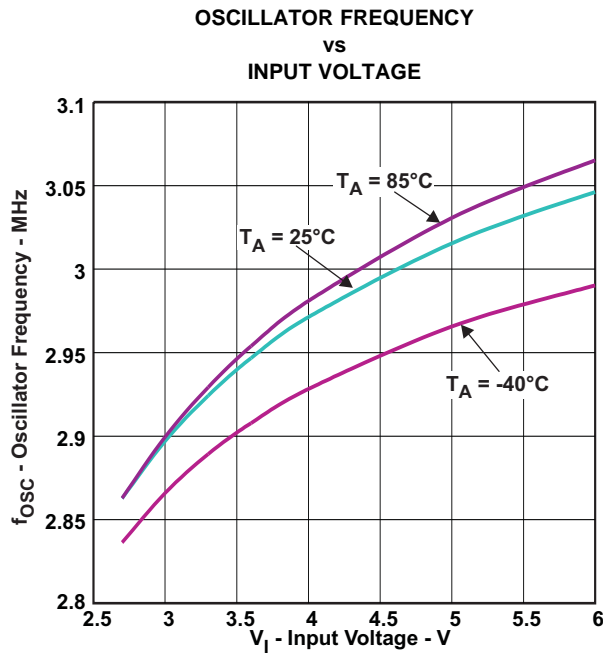


Figure 9.

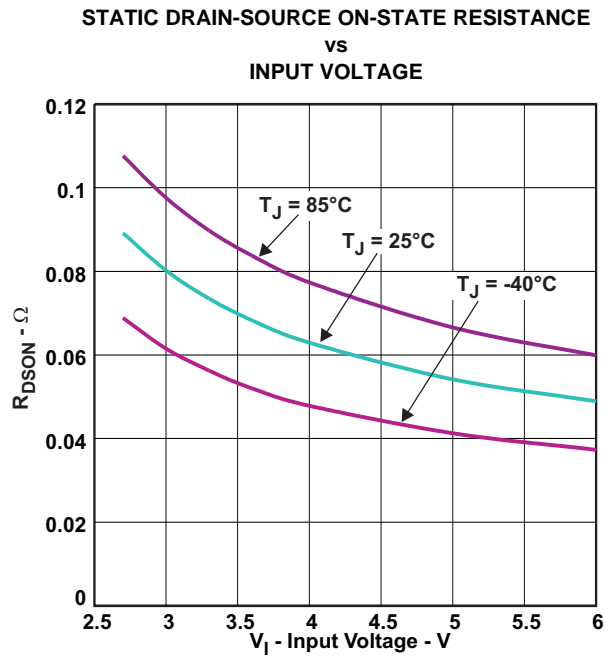


Figure 10. Low-Side Switch

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

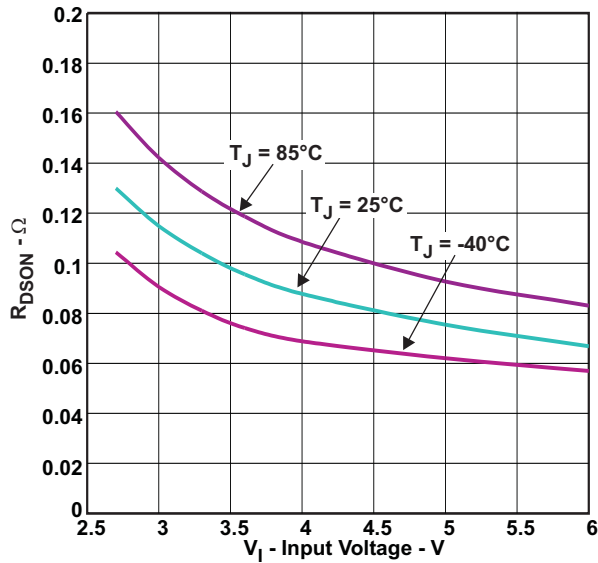


Figure 11. High-Side Switch

$R_{DISCHARGE}$
vs
INPUT VOLTAGE

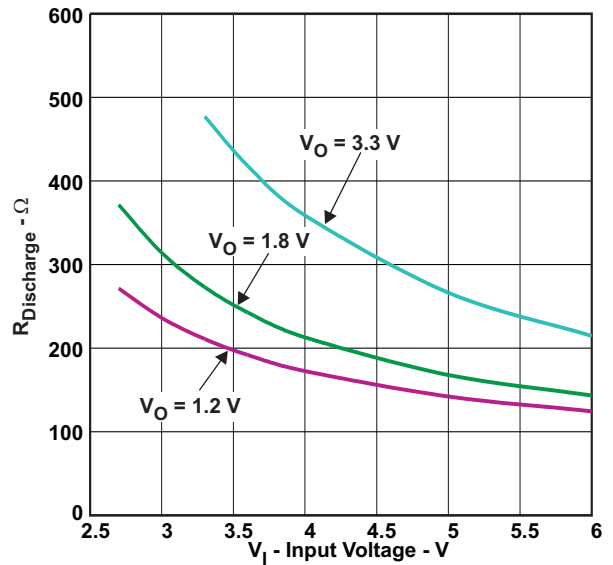
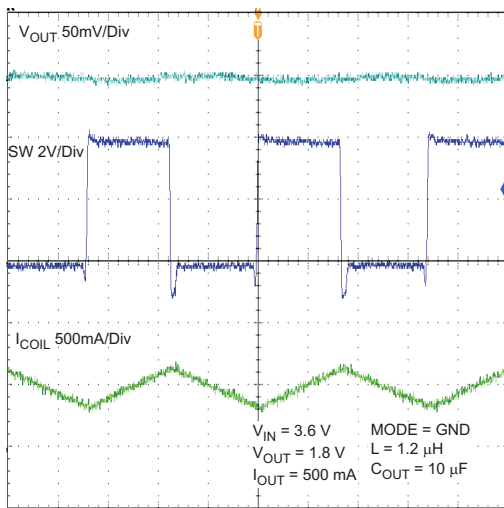
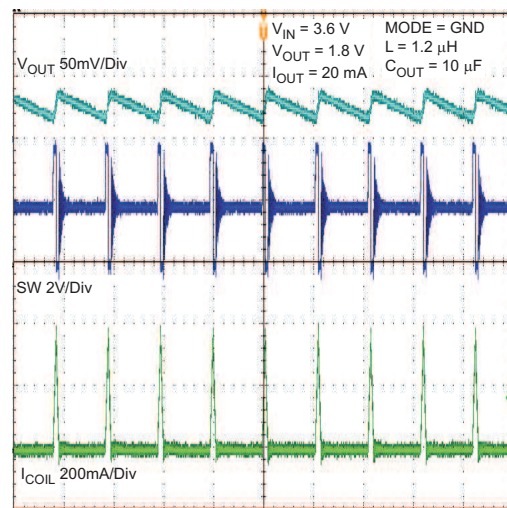


Figure 12.



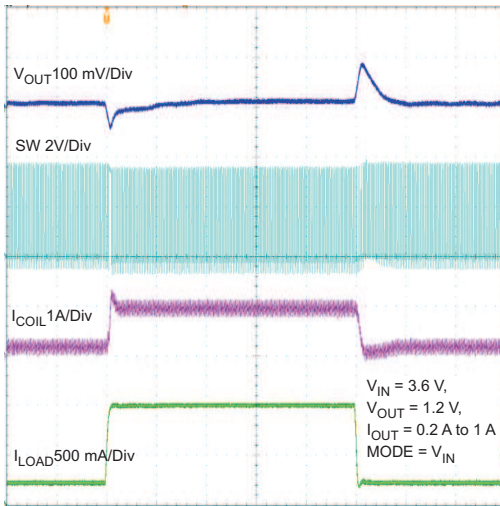
Time Base - 100ns/Div

Figure 13. Typical Operation (PWM Mode)



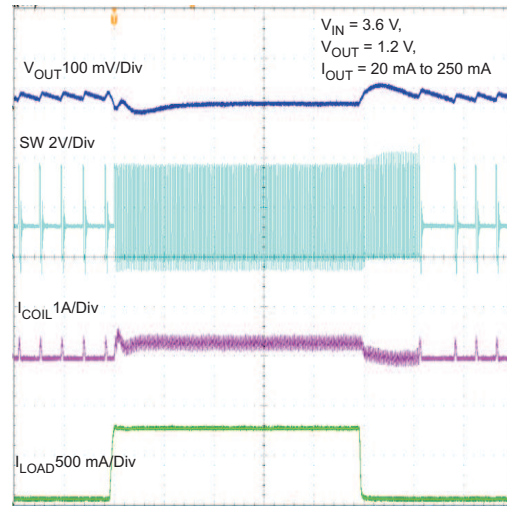
Time Base - 4 μ s/Div

Figure 14. Typical Operation (PFM Mode)



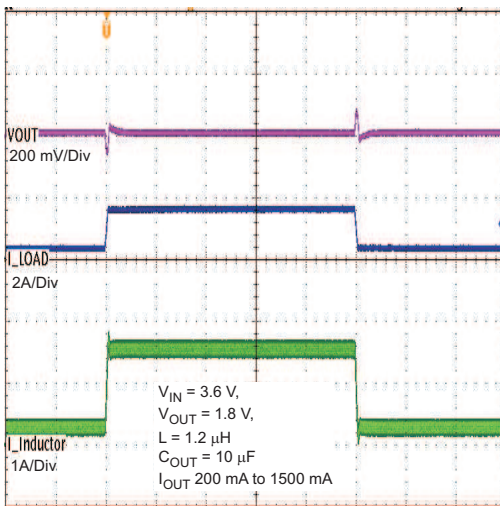
Time Base - 10 μ s/Div

Figure 15. Load Transient Response PWM Mode 0.2A To 1A



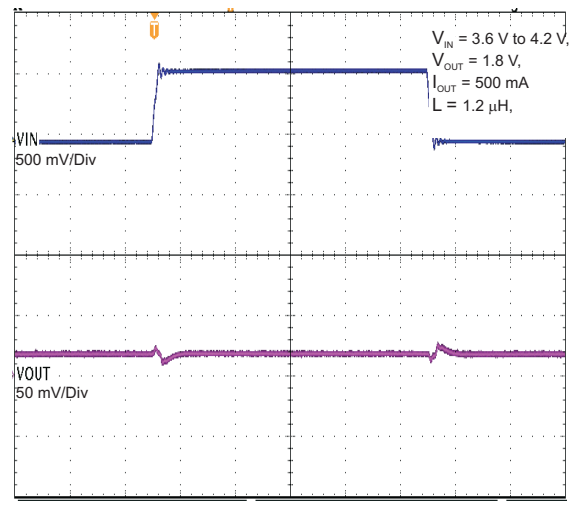
Time Base - 10 μ s/Div

Figure 16. Load Transient PFM Mode 20 mA to 250mA



Time Base - 100 μ s/Div

Figure 17. Load Transient Response 200 mA To 1500 mA



Time Base - 100 μ s/Div

Figure 18. Line Transient Response PWM Mode

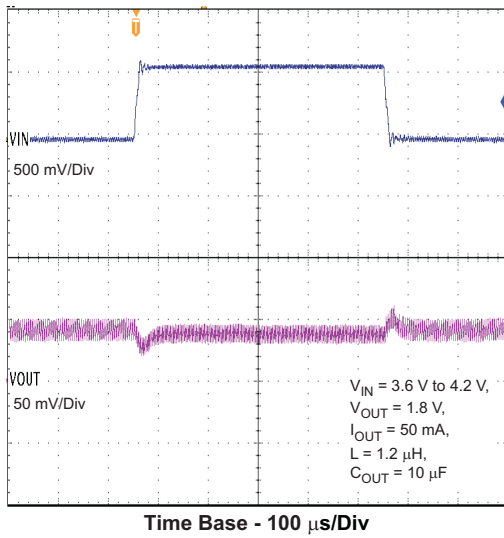


Figure 19. Line Transient PFM Mode

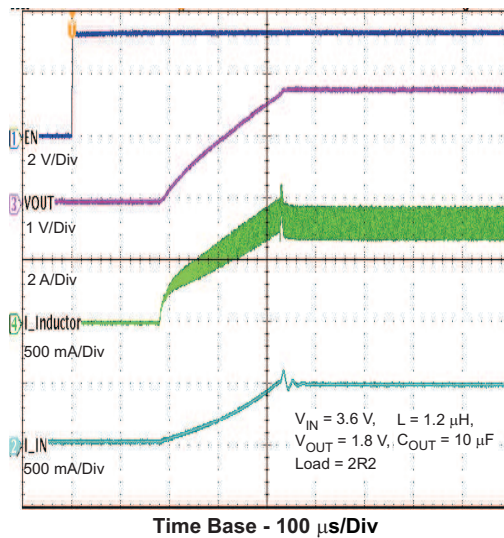


Figure 20. Start-Up Into Load – $V_{OUT} = 1.8 \text{ V}$

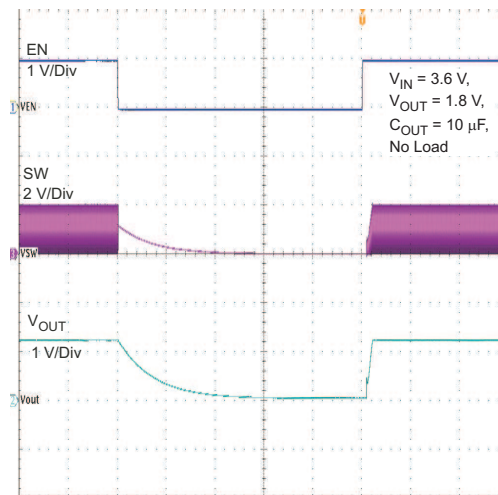


Figure 21. Output Discharge

DETAILED DESCRIPTION

OPERATION

The TLV62065-Q1 step-down converter operates with typically 3-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode, and operates then in pulse-frequency mode (PFM).

During PWM operation, the converter uses a unique fast-response voltage-mode controller scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

POWER SAVE MODE

Pulling the TLV62065-Q1 MODE pin low enables power-save mode. If the load current decreases, the converter enters power-save mode operation automatically. In power-save mode, the converter skips switching and operates with reduced frequency in the PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage-positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

In power-save mode, a PFM comparator monitors the output voltage. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal} + 1\%$, the device starts a PFM current pulse. For this, the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typ. 18- μ A current consumption.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold due to the load current.

The PFM mode is exited and PWM mode entered in case the output current can no longer be supported in PFM mode.

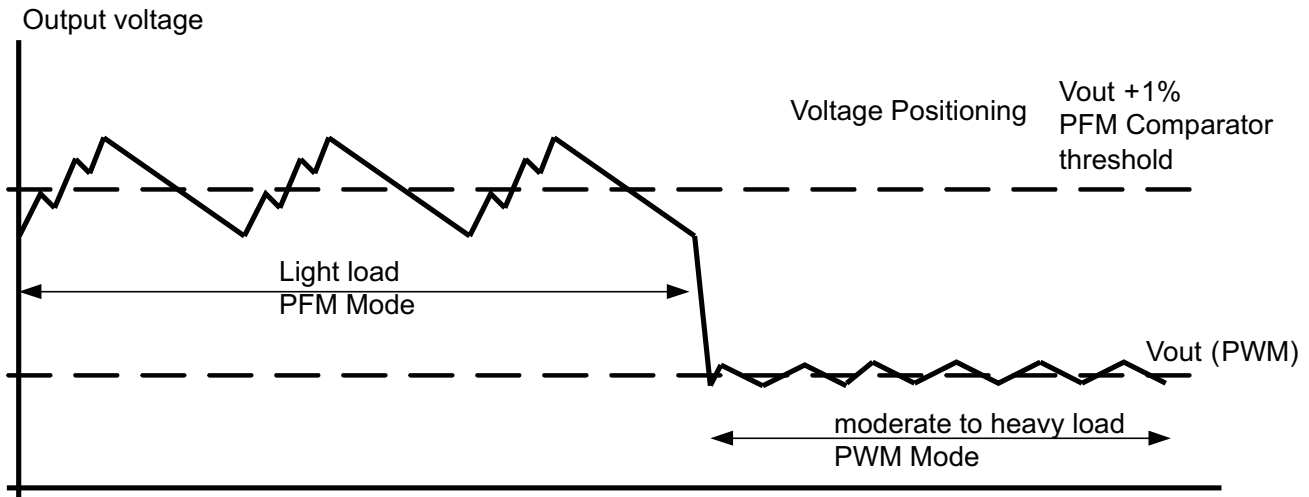


Figure 22. Power Save Mode Operation with automatic Mode transition

100% Duty Cycle Low-Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} , the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage differential. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{INmin} = V_{Omax} + I_{Omax} \times (R_{DS(on)max} + R_L)$$

With:

I_{Omax} = maximum output current

$R_{DS(on)max}$ = maximum P-channel switch $R_{DS(on)}$.

R_L = DC resistance of the inductor

V_{Omax} = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO} . The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is typically 1.78 V. The device starts operation once the rising V_{IN} trips the undervoltage lockout threshold V_{UVLO} again at typically 1.95 V.

Output Capacitor Discharge

With $EN = GND$, the device enters shutdown mode and disables all internal circuits. An internal resistor connects the SW pin to PGND to discharge the output capacitor. This feature ensures start-up with a discharged output capacitor once the converter is enabled again and prevents *floating* charge on the output capacitor. The output voltage ramps up monotonically, starting from 0 V.

MODE SELECTION

The MODE pin allows mode selection between forced PWM mode and power-save mode.

Connecting this pin to GND enables the power-save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

ENABLE

The device is enabled by setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches 95% of its nominal value within t_{START} of typically 500 μs after the device has been enabled. The EN input can be used to control power sequencing in a system with various dc-dc converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND via an internal resistor to discharge the output.

SOFT START

The TLV62065-Q1 has an internal soft-start circuit that controls the ramp-up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold, V_{UVLO} , the output voltage ramps up from 5% to 95% of its nominal value within t_{Ramp} of typ. 250 μs .

This limits the inrush current in the converter during start-up and prevents possible input-voltage drops when a battery or high-impedance power source is used.

During soft start, the switch current limit is reduced to 1/3 of its nominal value, I_{LIMF} , until the output voltage reaches 1/3 of its nominal value. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF} .

INTERNAL CURRENT LIMIT / FOLD-BACK CURRENT LIMIT FOR SHORT-CIRCUIT PROTECTION

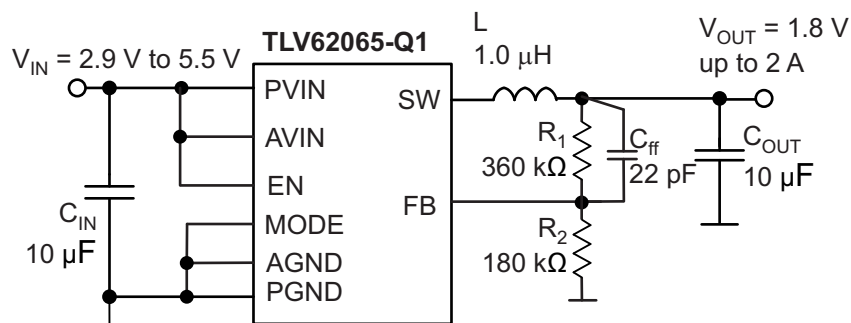
During normal operation, the high-side and low-side MOSFET switches are protected by their current limits, I_{LIMF} . Once the high-side MOSFET switch reaches its current limit, it is turned off and the low-side MOSFET switch is turned on. The high-side MOSFET switch can only turn on again once the current in the low-side MOSFET switch decreases below its current limit, I_{LIMF} . The device is capable of providing peak inductor currents up to its internal current limit I_{LIMF} .

As soon as the switch-current limits are hit and the output voltage falls below 1/3 of the nominal output voltage due to an overload or short-circuit condition, the foldback current limit is enabled. In this case, the switch-current limit is reduced to 1/3 of the nominal value, I_{LIMF} .

Because the short-circuit protection is enabled during start-up, the device does not deliver more than 1/3 of its nominal current limit, I_{LIMF} , until the output voltage exceeds 1/3 of the nominal output voltage. This must be considered when a load which acts as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_{J} , exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation with a soft start once the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

Figure 23. TLV62065-Q1 1.8V Adjustable Output Voltage Configuration
OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{\text{OUT}} = V_{\text{REF}} \times \left(1 + \frac{R_1}{R_2} \right)$$

with an internal reference voltage V_{REF} typically 0.6 V.

To minimize the current through the feedback divider network, R_2 should be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 should not exceed approximately 1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_{ff} is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} place a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_c = \frac{1}{2 \times \pi \times R_2 \times C_{\text{ff}}} = 35\text{kHz}$$

$$C_{\text{ff}} = \frac{1}{2 \times \pi \times R_2 \times 35\text{kHz}}$$

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The internal compensation network of TLV62065-Q1 is optimized for an LC output filter with a corner frequency of:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(1\mu\text{H} \times 10\mu\text{F})}} = 50\text{kHz}$$

The part operates with nominal inductors of 1 μH to 1.2 μH and with 10 μF to 22 μF small X5R and X7R ceramic capacitors. See the lists of inductors and capacitors. The part is optimized for a 1- μH inductor and 10- μF output capacitor.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O .

[Equation 1](#) calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with [Equation 2](#). This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \quad (1)$$

$$I_{L_{\text{max}}} = I_{\text{outmax}} + \frac{\Delta I_L}{2} \quad (2)$$

where:

f = Switching frequency (3 MHz typical)

L = Inductor value

ΔI_L = Peak-to-peak inductor ripple current

$I_{L_{\text{max}}}$ = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch-current limit $I_{L_{\text{LIMF}}}$ of the converter.

The total losses of the coil have a strong impact on the efficiency of the dc-dc conversion and consist of both the losses in the dc resistance $R_{(\text{DC})}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 2. List of Inductors

DIMENSIONS [mm]	INDUCTANCE μH	INDUCTOR TYPE	SUPPLIER
3.2 x 2.5 x 1 max.	1	LQM32PN (MLCC)	Murata
3.7 x 4 x 1.8 max.	1	LQH44 (wire wound)	Murata
4 x 4 x 2.6 max.	1.2	NRG4026T (wire wound)	Taiyo Yuden
3.5 x 3.7 x 1.8 max.	1.2	DE3518 (wire wound)	TOKO

Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TLV62065-Q1 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V- and Z5U-dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications, a nominal 10- μ F or 22- μ F capacitor is suitable. In small ceramic capacitors, the dc-bias effect decreases the effective capacitance. Therefore a 22- μ F capacitor can be used for output voltages higher than 2 V; see the list of capacitors, [Table 3](#).

In case additional ceramic capacitors in the supplied system are connected to the output of the dc-dc converter, the output capacitor C_{OUT} must be decreased in order not to exceed the recommended effective capacitance range. In this case, a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMS\text{Cout}} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. For most applications a 10- μ F ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE [mm]	SUPPLIER
10 μ F	GRM188R60J106M	0603: 1.6 × 0.8 × 0.8	Murata
22 μ F	GRM188R60G226M	0603: 1.6 × 0.8 × 0.8	Murata
22 μ F	CL10A226MQ8NRNC	0603: 1.6 × 0.8 × 0.8	Samsung
10 μ F	CL10A106MQ8NRNC	0603: 1.6 × 0.8 × 0.8	Samsung

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signal

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter, or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or wrong L-C output filter combinations. As a next step in the evaluation of the regulation loop, the transient response of the load is tested. During the time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times ESR$, where ESR is the effective series resistance of C_{OUT} . $\Delta I_{(LOAD)}$ begins to charge or discharge C_O , generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode at medium-to-high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

LAYOUT CONSIDERATIONS

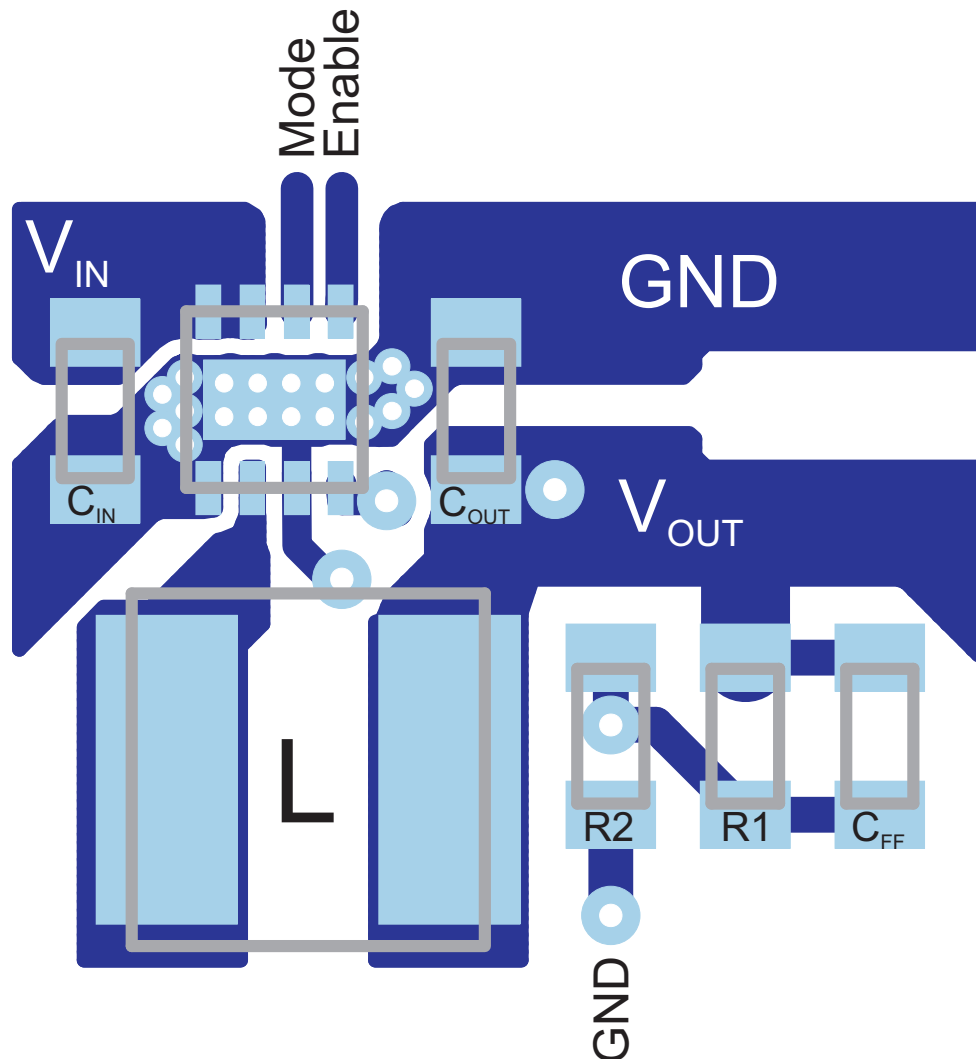


Figure 24. PCB Layout

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI and thermal problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor as well as the inductor and output capacitor should be placed as close as possible to the IC pins.

Connect the AGND and PGND pins of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common power node (PGND), and a different node (AGND) for the signal, to minimize the effects of ground noise. The FB divider network should be connected directly to the output capacitor and the FB line must be routed away from noisy components and traces (for example, the SW line).

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. For good thermal performance PCB design of at least four layers is recommended. The thermal pad of the IC must be soldered on the power pad area on the PCB to achieve proper thermal connection. Additionally, for good thermal performance, the thermal pad on the PCB must be connected to an inner GND plane with sufficient via connections. See the documentation of the evaluation kit.

TLV62065-Q1

ZHCS783A – JANUARY 2012 – REVISED MARCH 2012

www.ti.com.cn

Revision History

The following table summarizes the TLV62065-Q1 data sheet versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
*	SLVSB92	January 2011	See ⁽¹⁾
A	SLVSB92A	March 2012	See ⁽²⁾

(1) TLV62065-Q1 Data Sheet, (SLVSB92) - Initial release.

(2) TLV62065-Q1 Data Sheet, (SLVSB92A):

- (a) [特性](#) - Update automotive qualification description and add temperature grade
- (b) [ABSOLUTE MAXIMUM RATINGS](#) - Update Absolute Maximum Ratings
- (c) [ELECTRICAL CHARACTERISTICS](#) - Update Electrical Characteristics - Shutdown current max rating

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62065TDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SCD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV62065-Q1 :

- Catalog: [TLV62065](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62065TDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

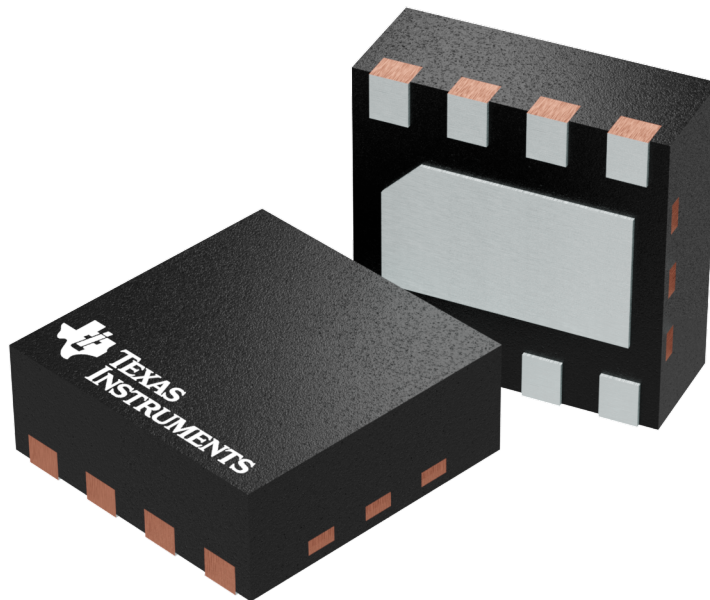
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62065TDSGRQ1	WSON	DSG	8	3000	195.0	200.0	45.0

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

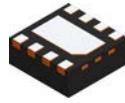
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4208210/C

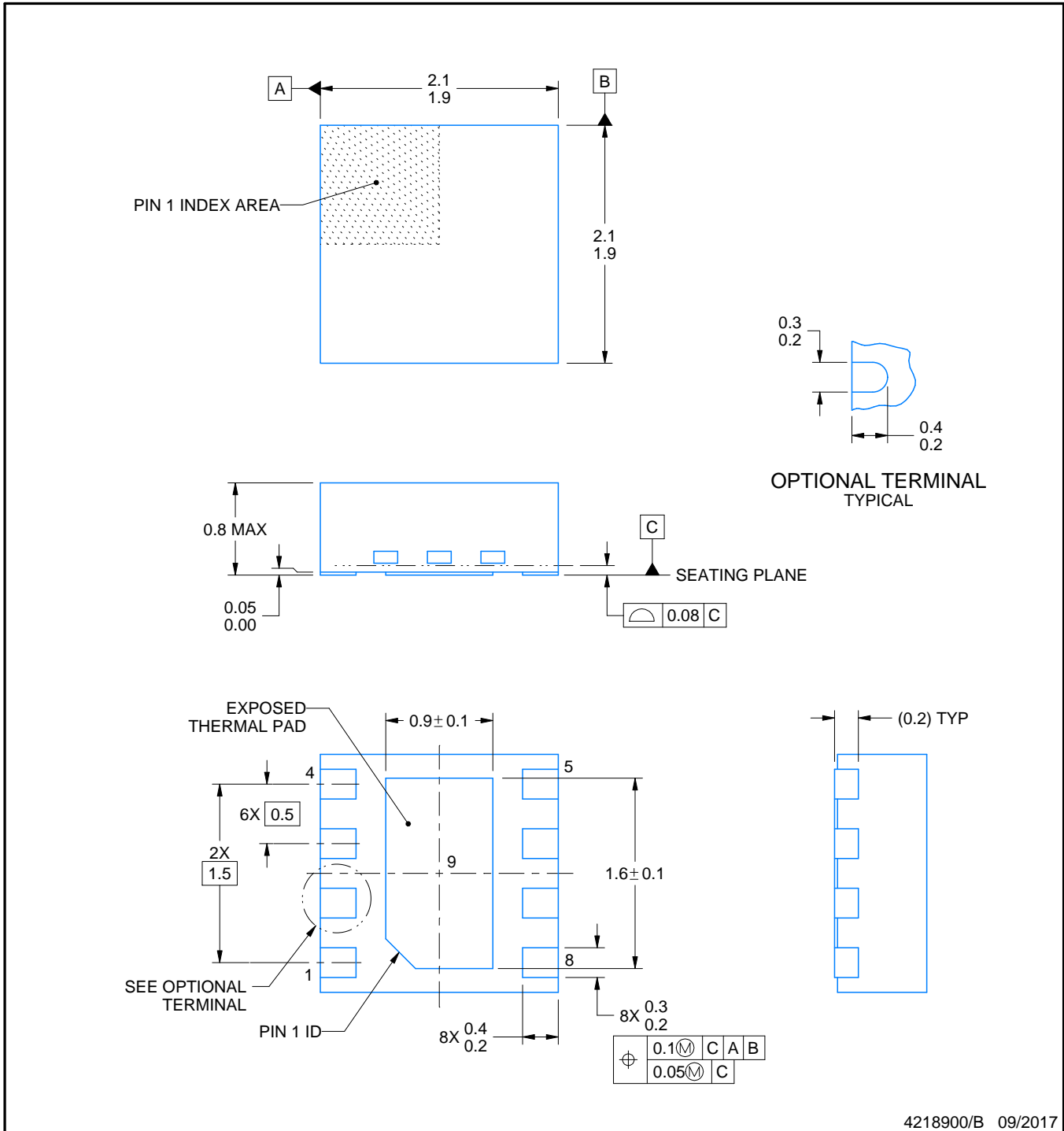
DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218900/B 09/2017

NOTES:

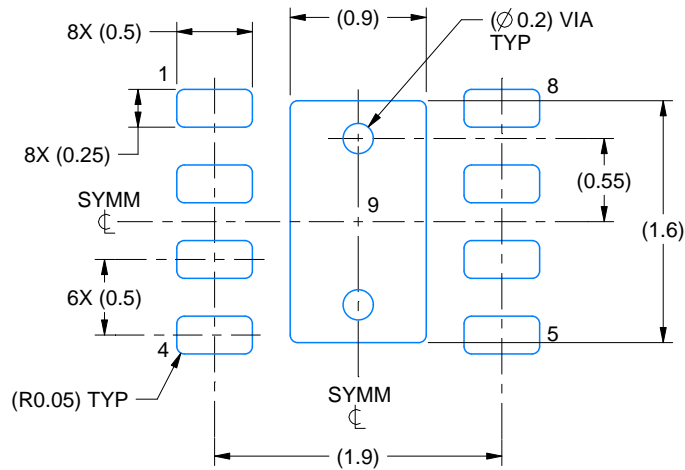
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

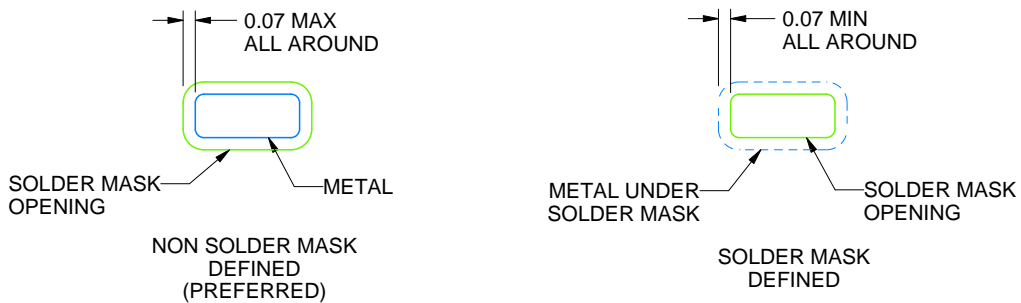
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与美国 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司